


# P45U V10

## GP106 8GB/4GB GDDR5, 256b, 256Mx32/128MX32 Tall DVI-D + HDMI+ DP

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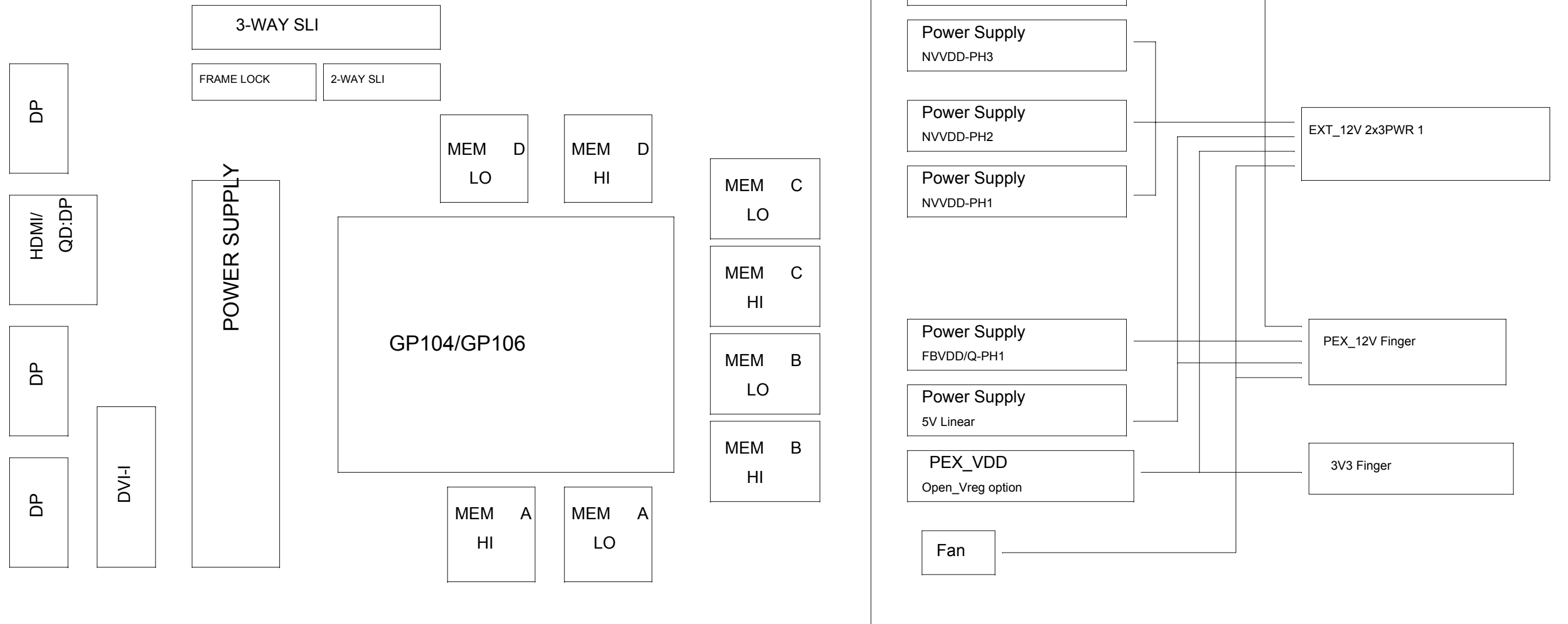
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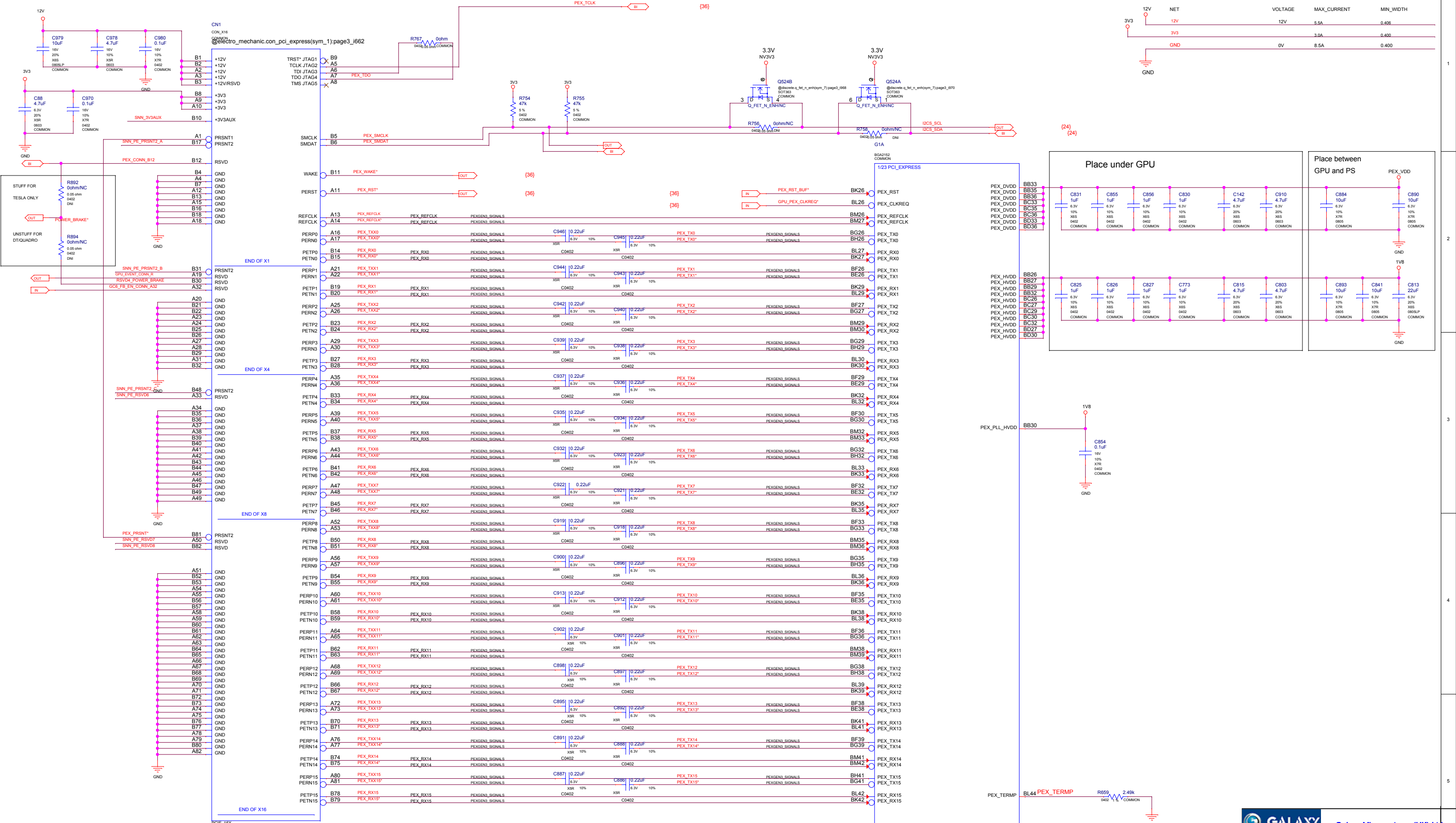
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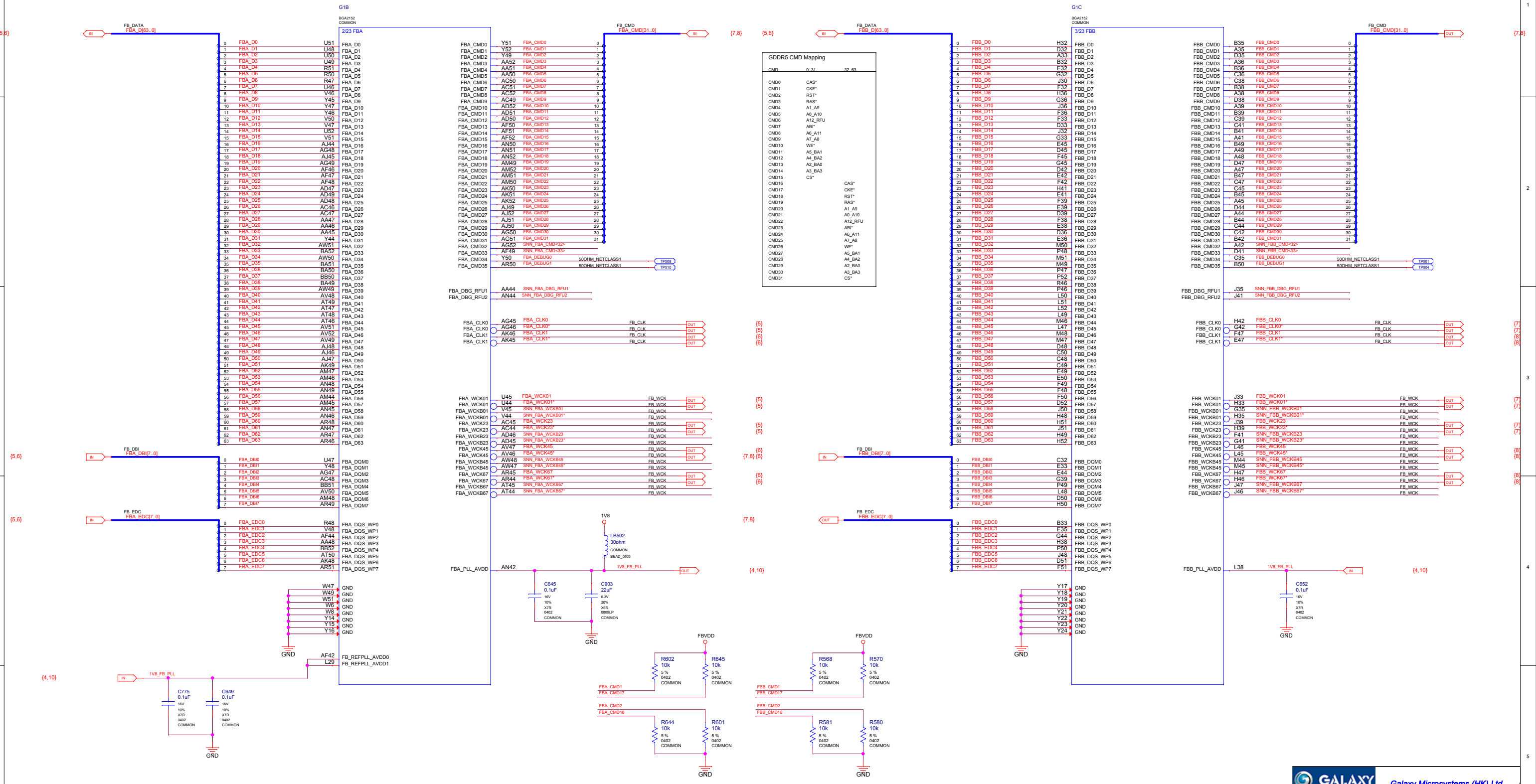
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**GDDR5 CMD Mapping**

CMD	0..31	32..63
CM00	CAS*	
CM01	CKE*	
CM02	RST*	
CM03	RAS*	
CM04	A1_A9	
CM05	A0_A10	
CM06	A12_RFU	
CM07	AB*	
CM08	AB_A11	
CM09	AT_A8	
CM10	WE*	
CM11	AS_BA1	RAS*
CM12	AB_BA2	
CM13	A2_BA0	
CM14	A3_BA3	
CM15	CS*	
CM16		CAS*
CM17		CKE*
CM18		RST*
CM19		RAS*
CM20		A1_A9
CM21		A0_A10
CM22		A12_RFU
CM23		AB*
CM24		AB_A11
CM25		AT_A8
CM26		WE*
CM27		AS_BA1
CM28		AB_BA2
CM29		A2_BA0
CM30		A3_BA3
CM31		CS*

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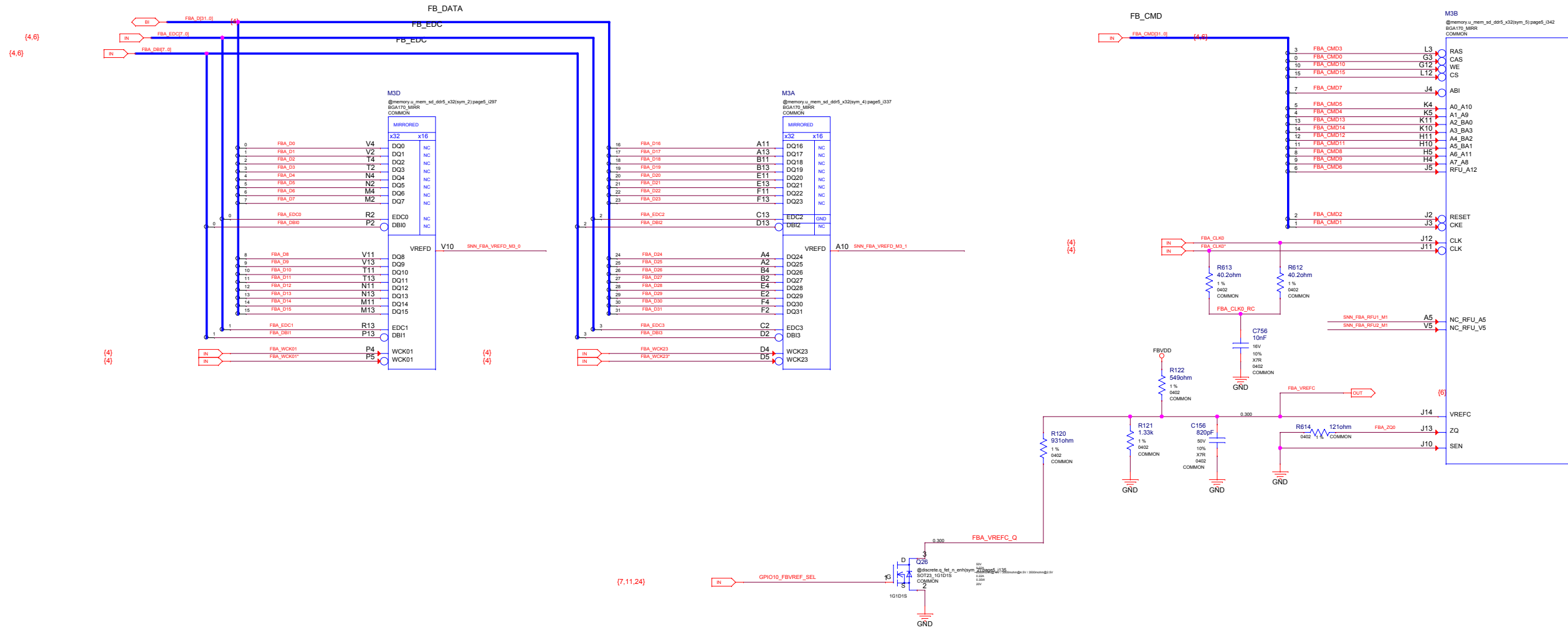
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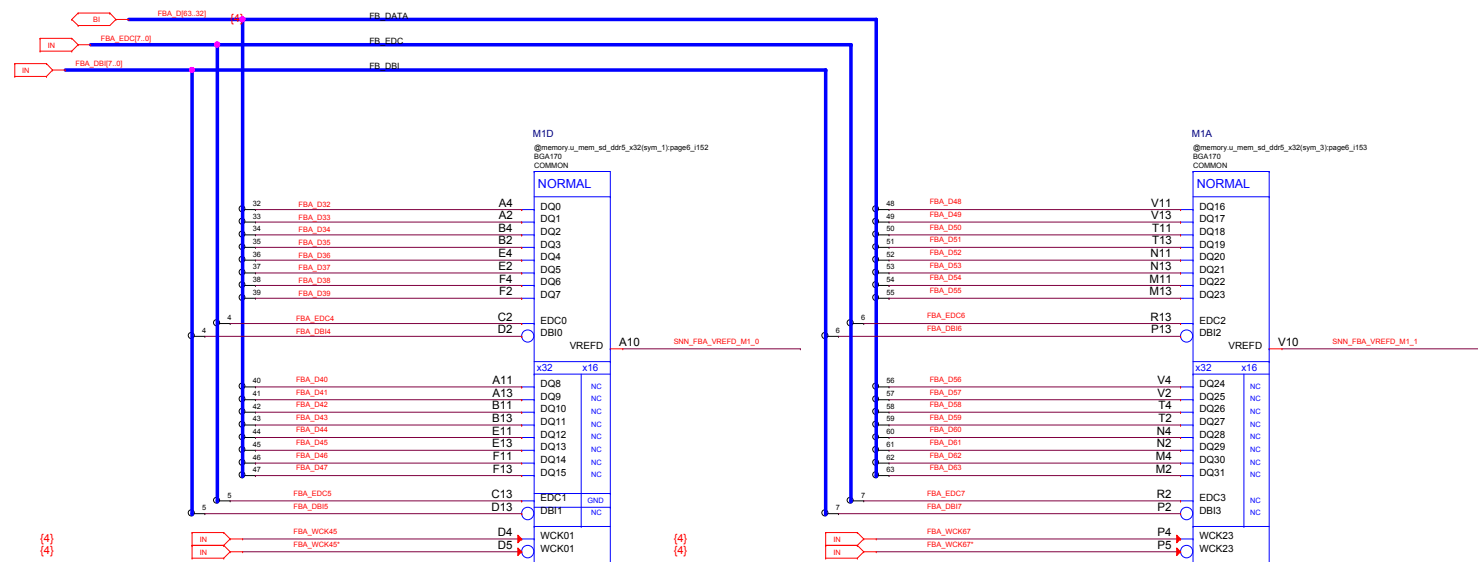
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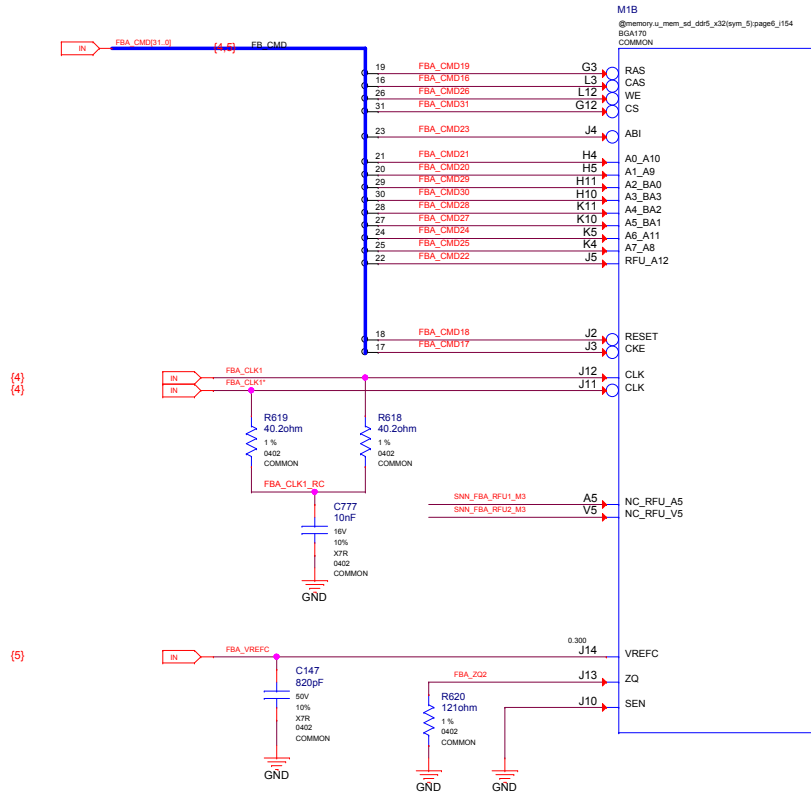
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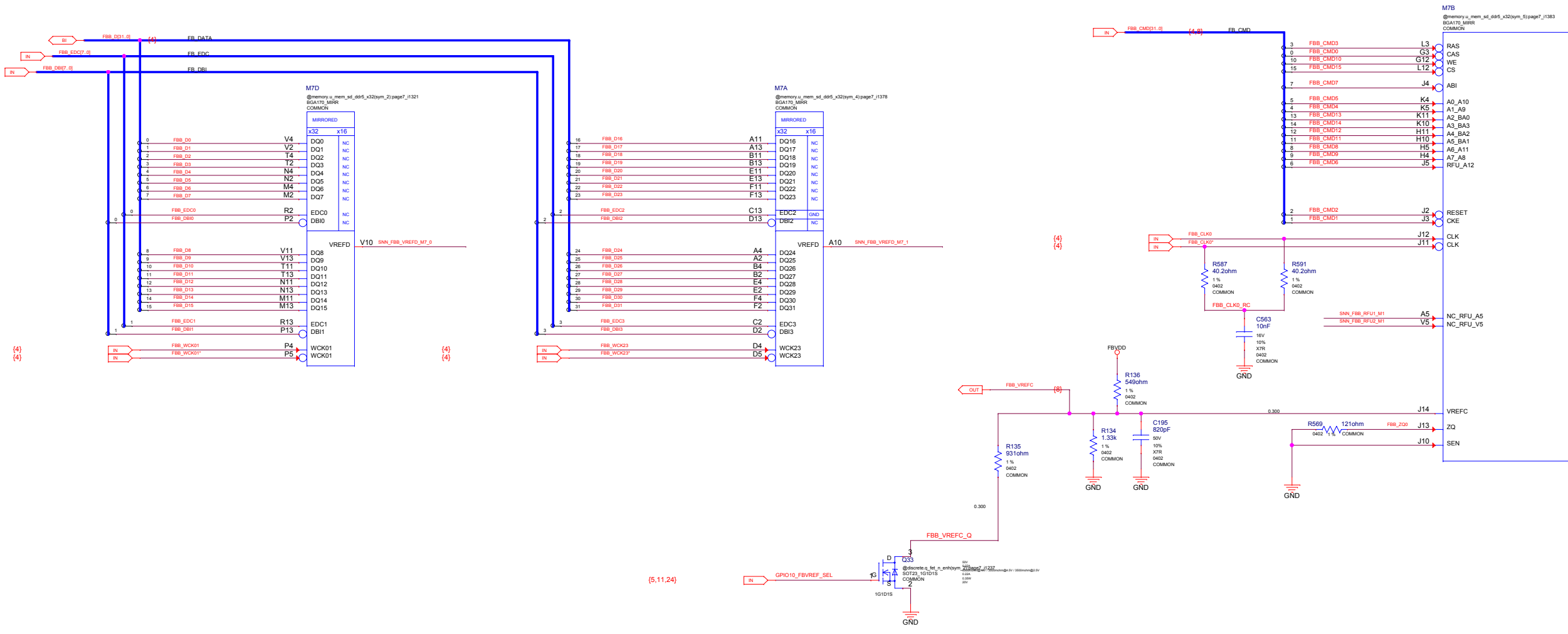
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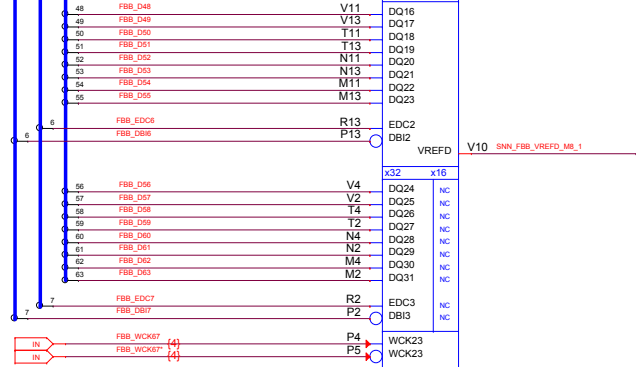
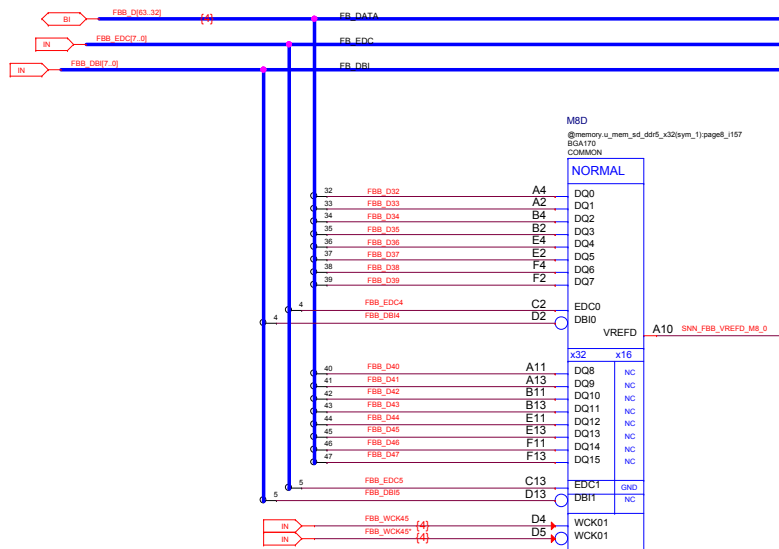
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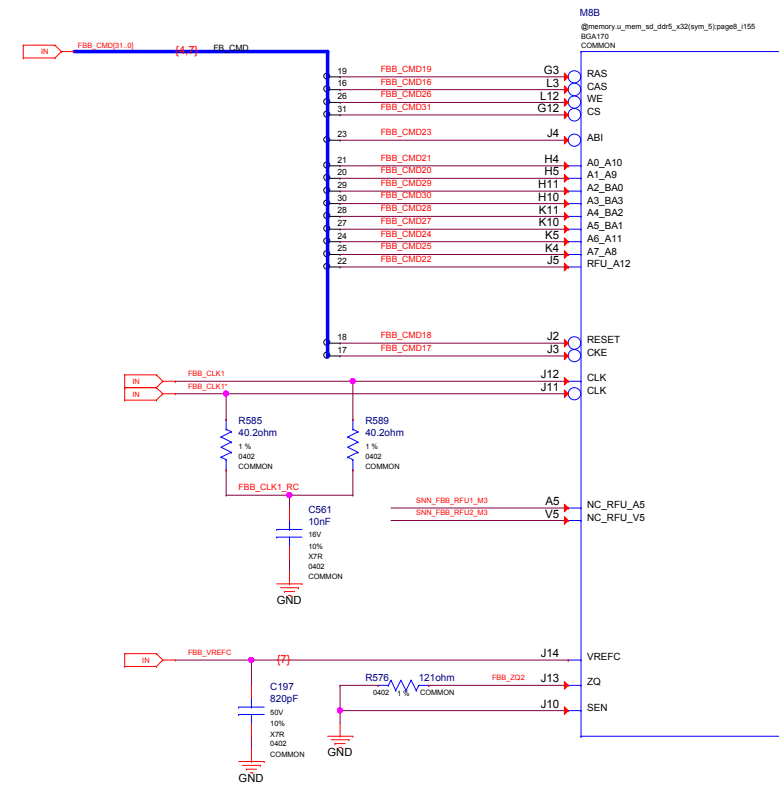
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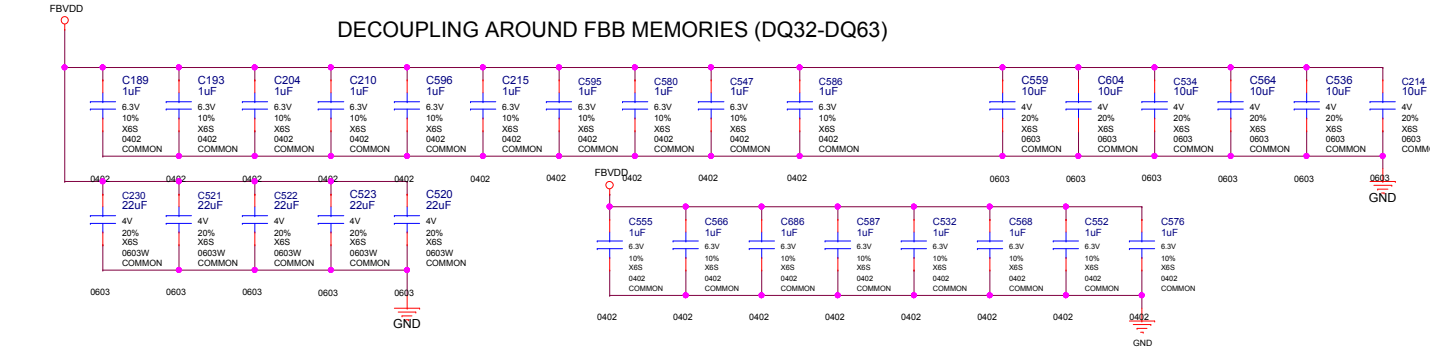
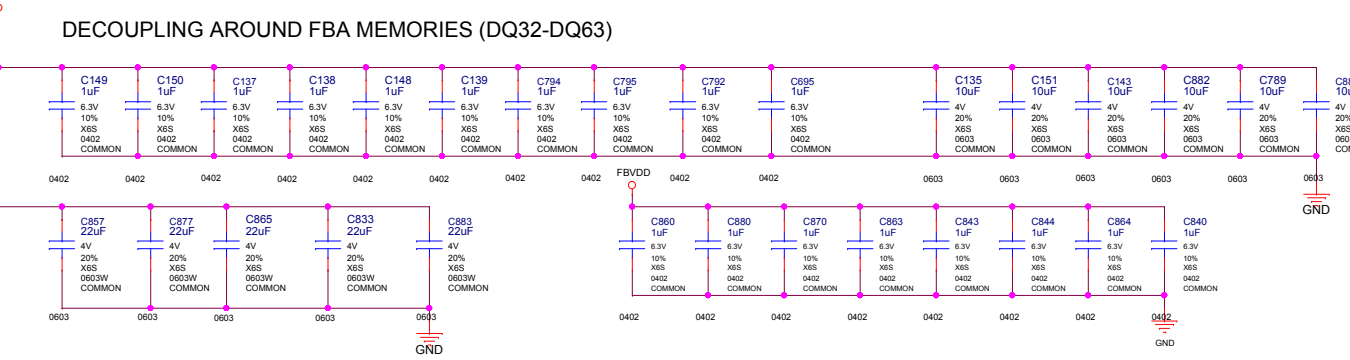
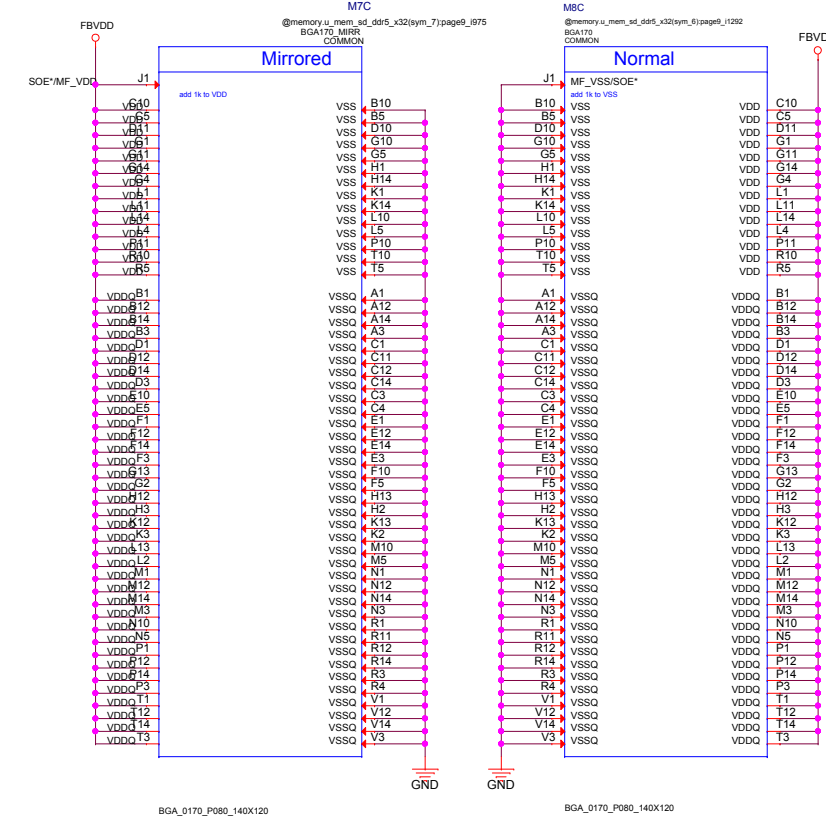
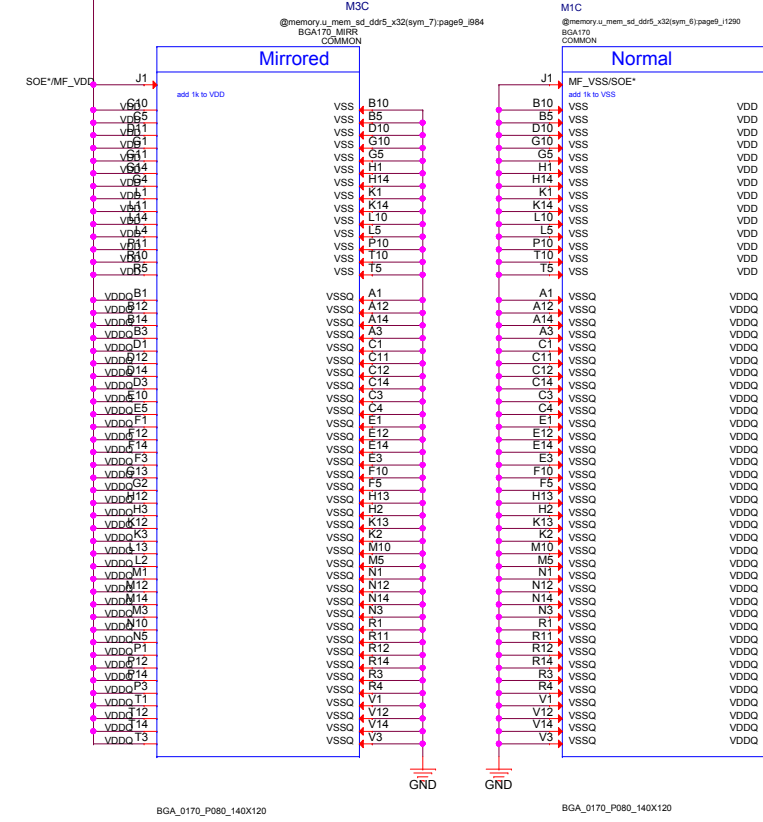
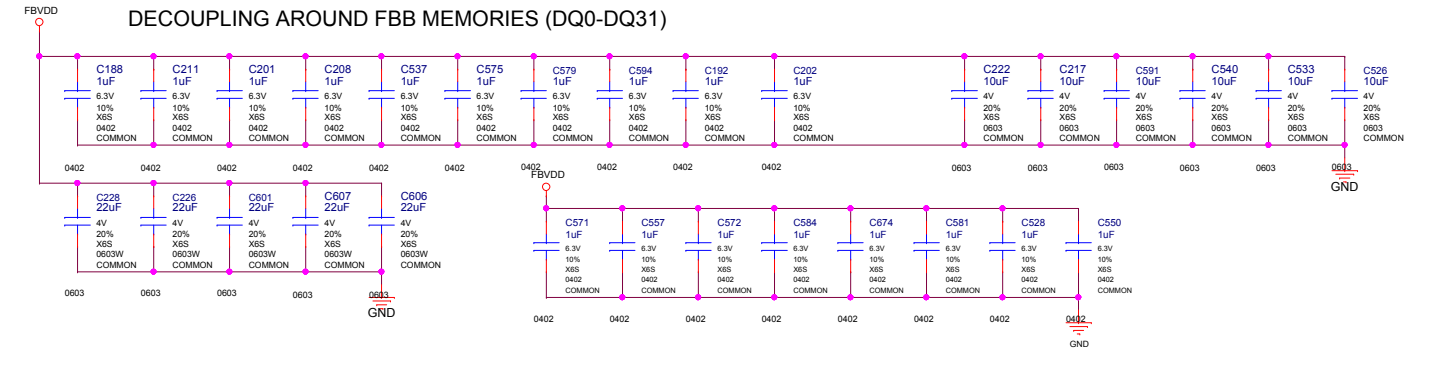
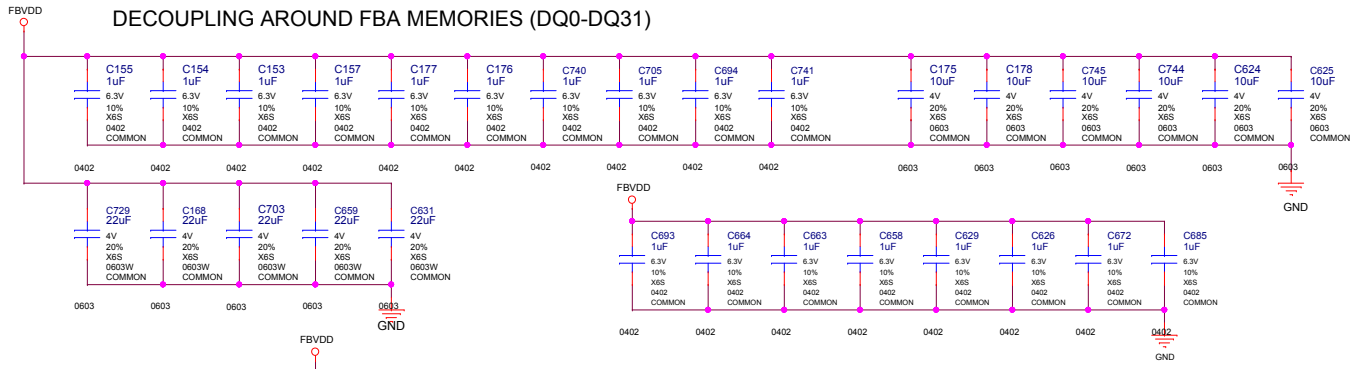
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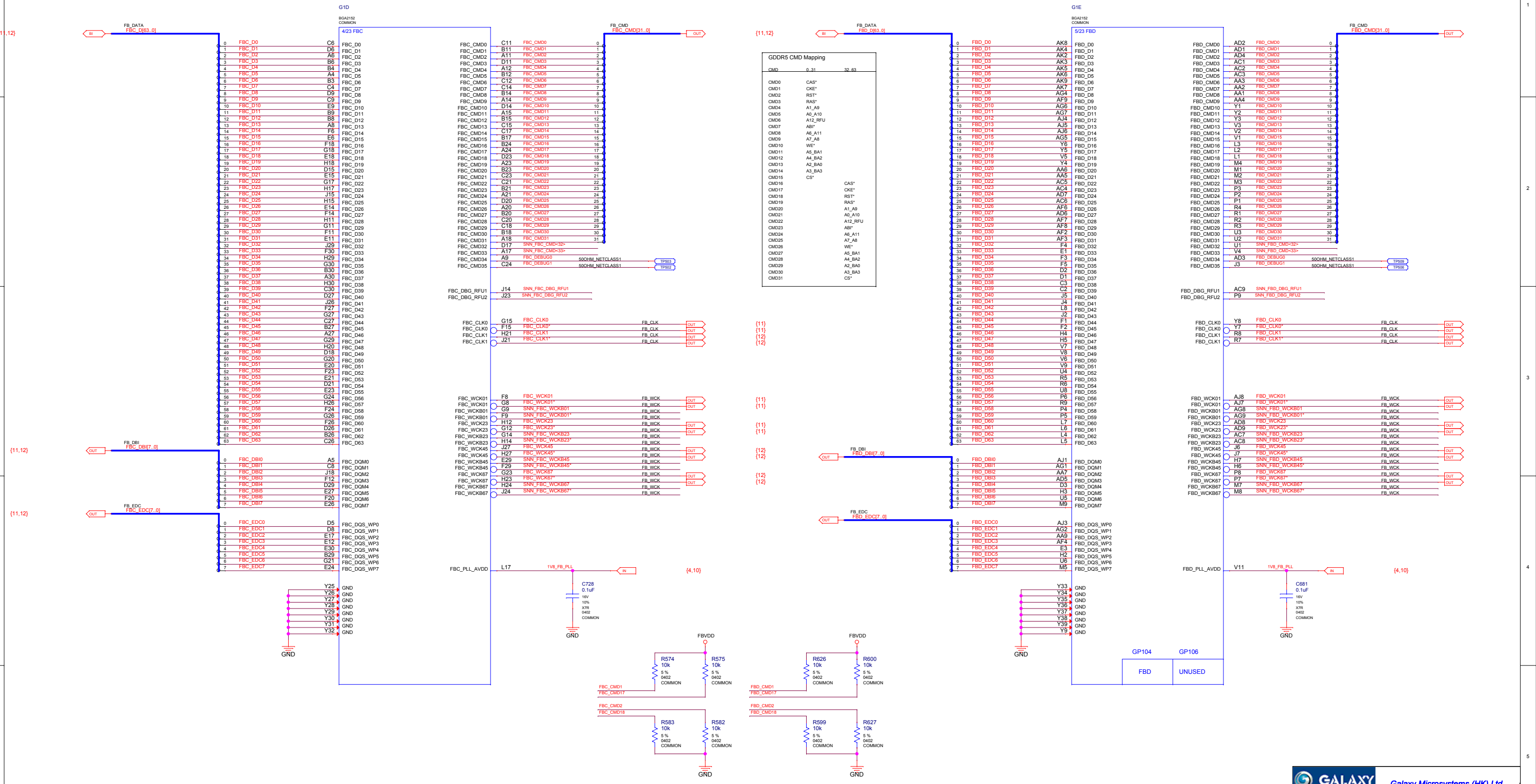
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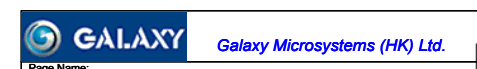
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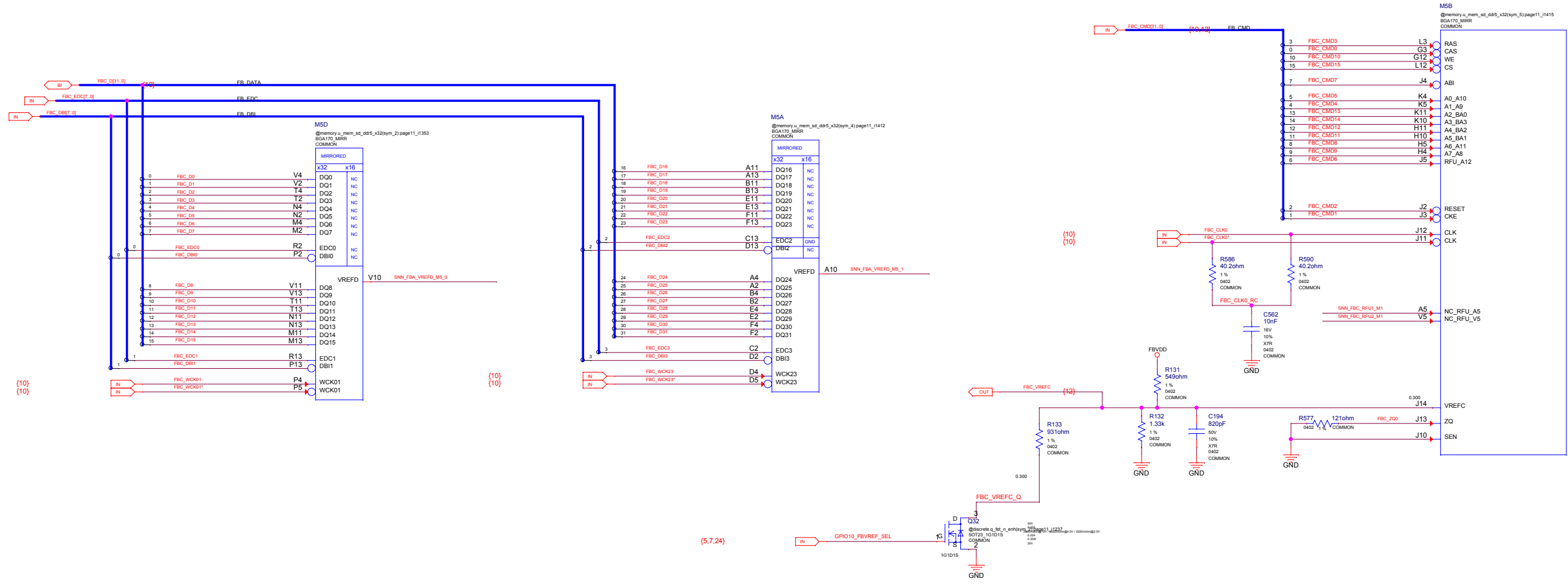
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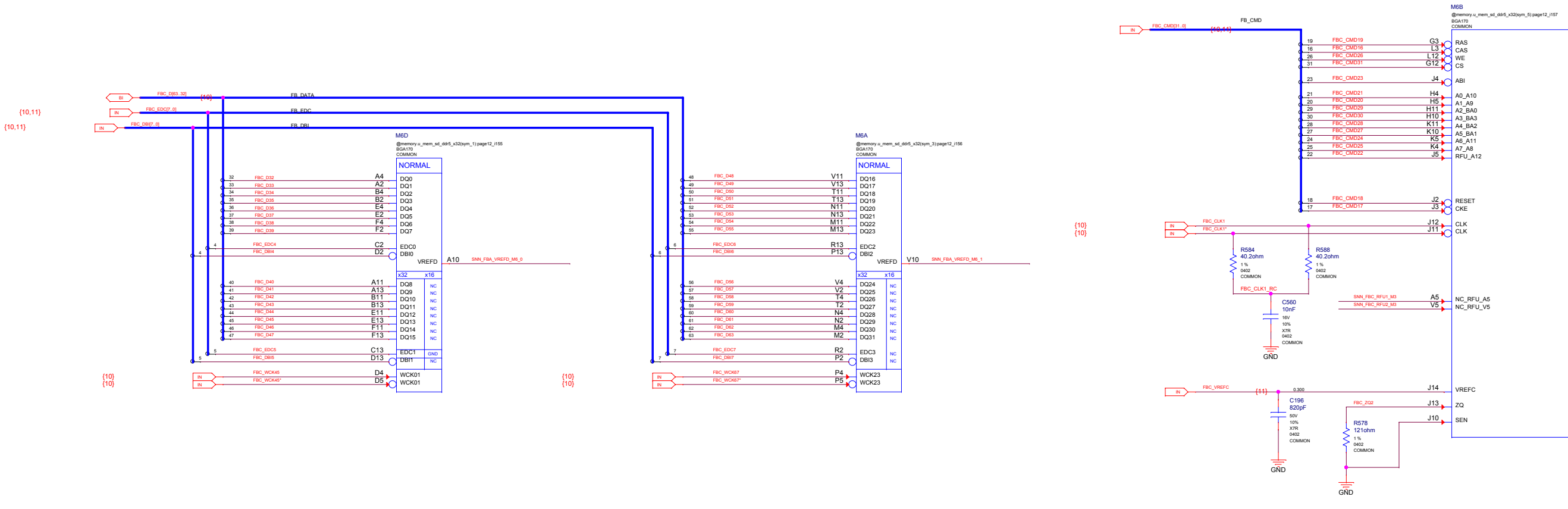
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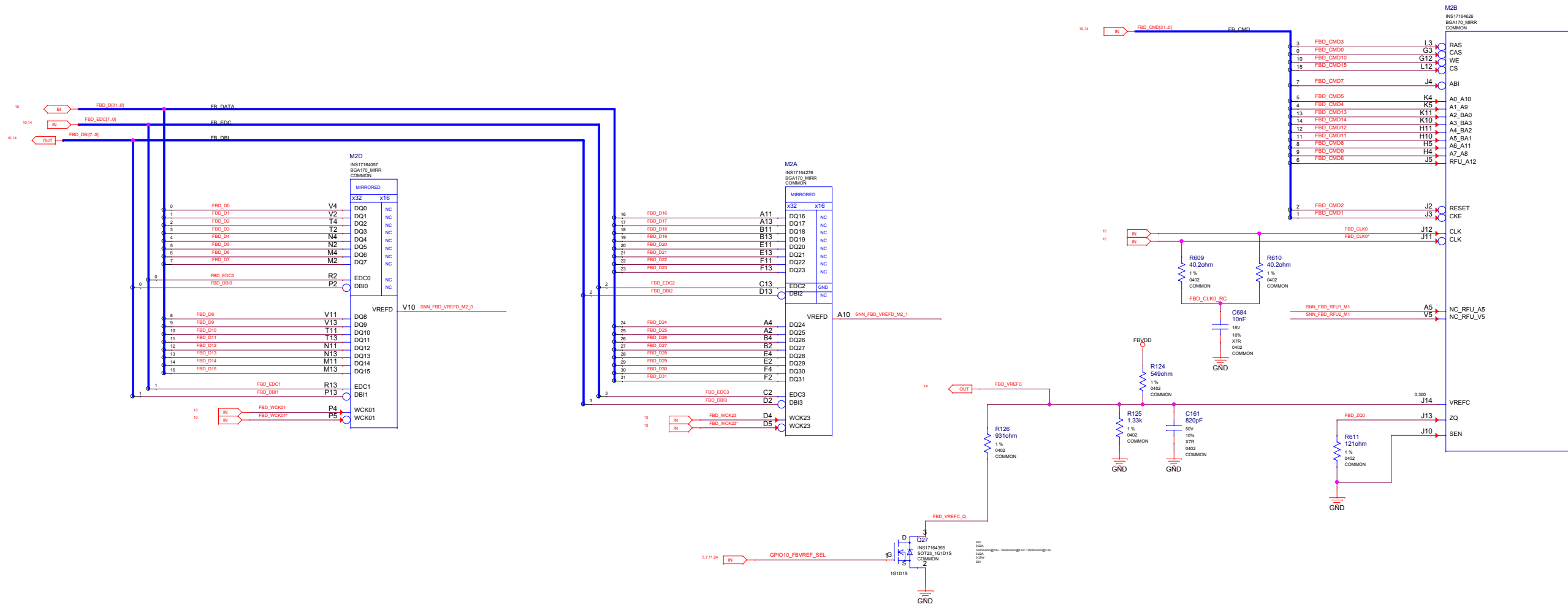
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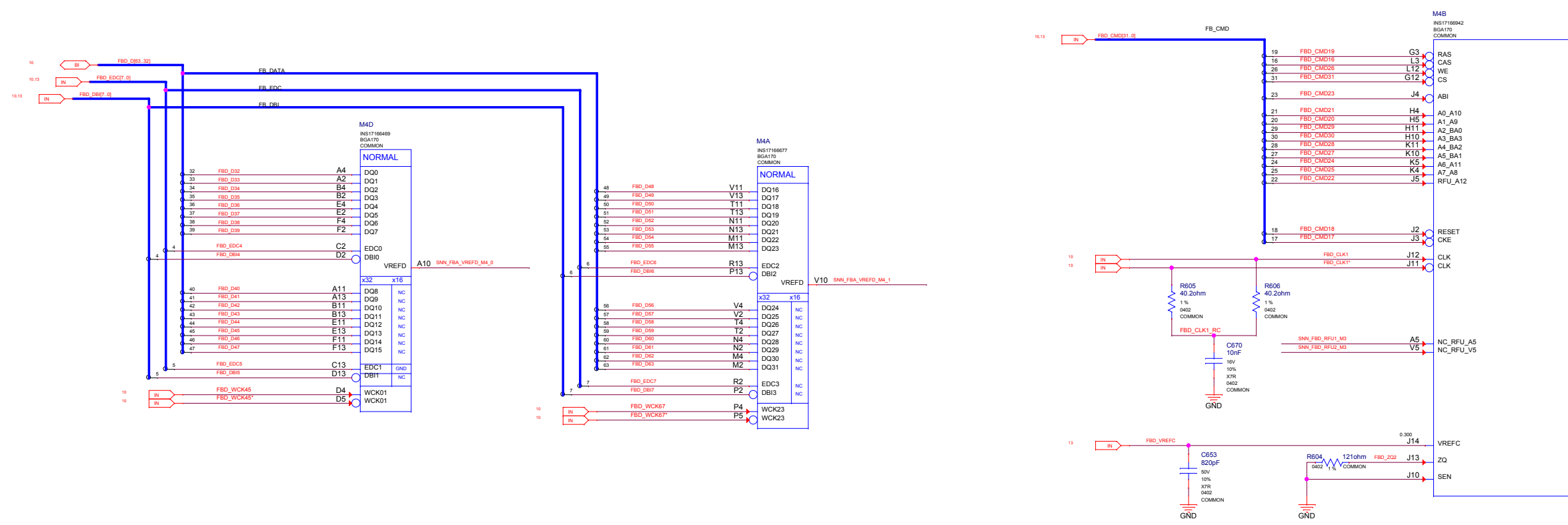
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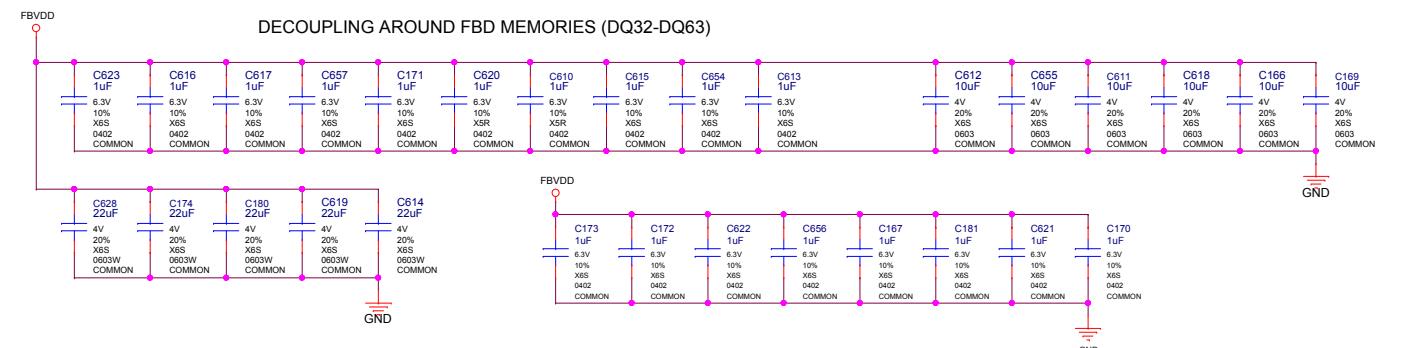
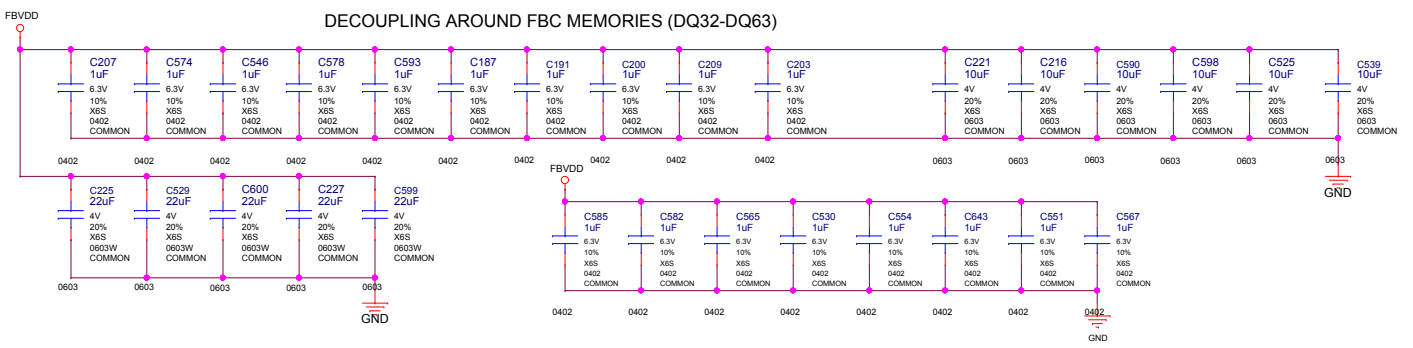
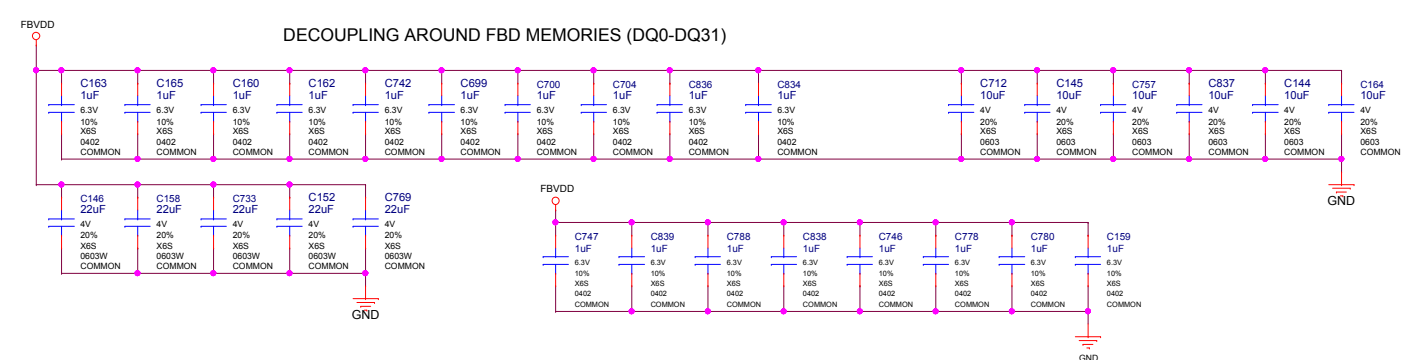
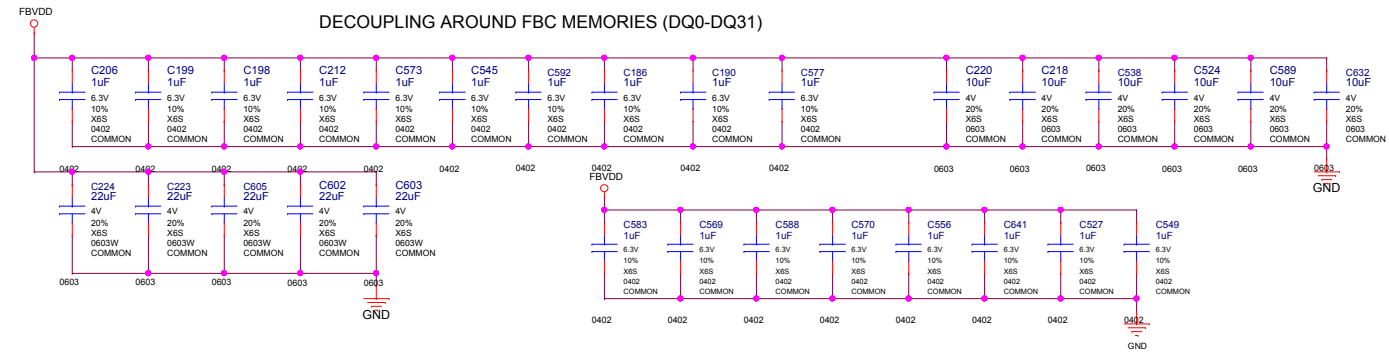
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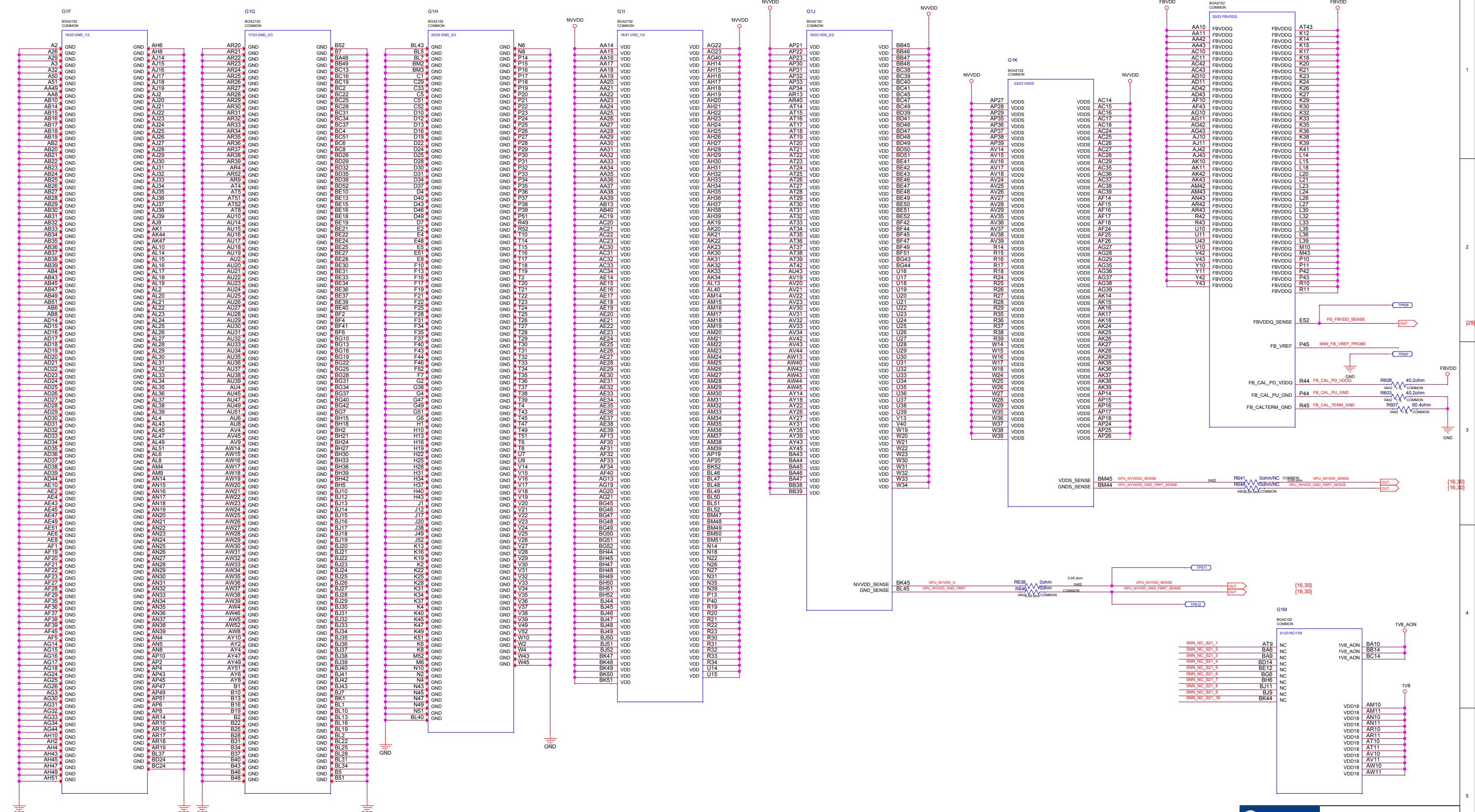
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ASSEMBLY PAGE DETAIL	<ASSEMBLY_DESCRIPTION> GPU PWR & GND
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**GALAXY** Galaxy Microsystems (HK) Ltd.

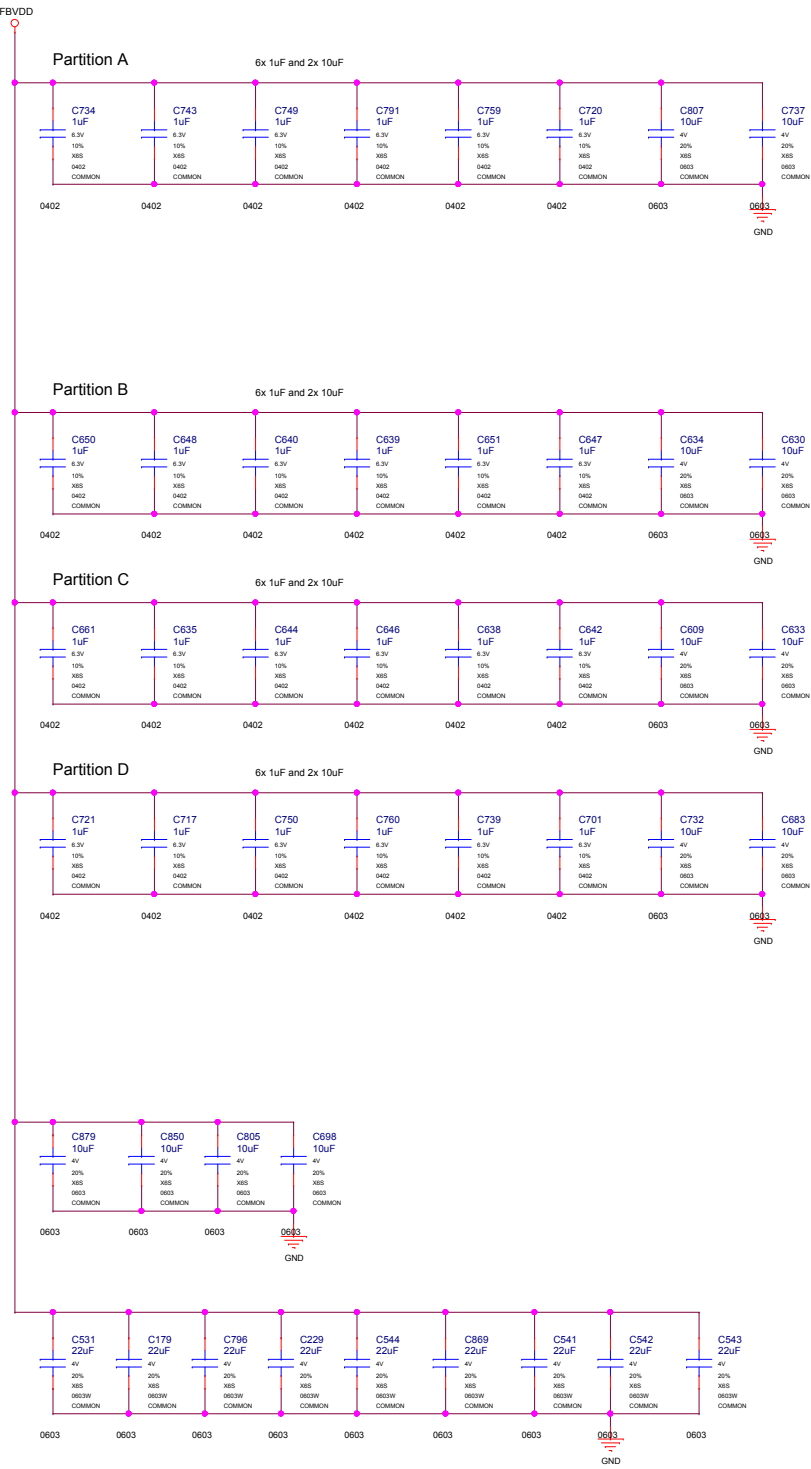
Page Name: GPU PWR & GND

Size: Custom	Project Name: P45U	Design By: Carson	Rev: V10
Date: Thursday, December 28, 2017	Sheet: 16	of 37	

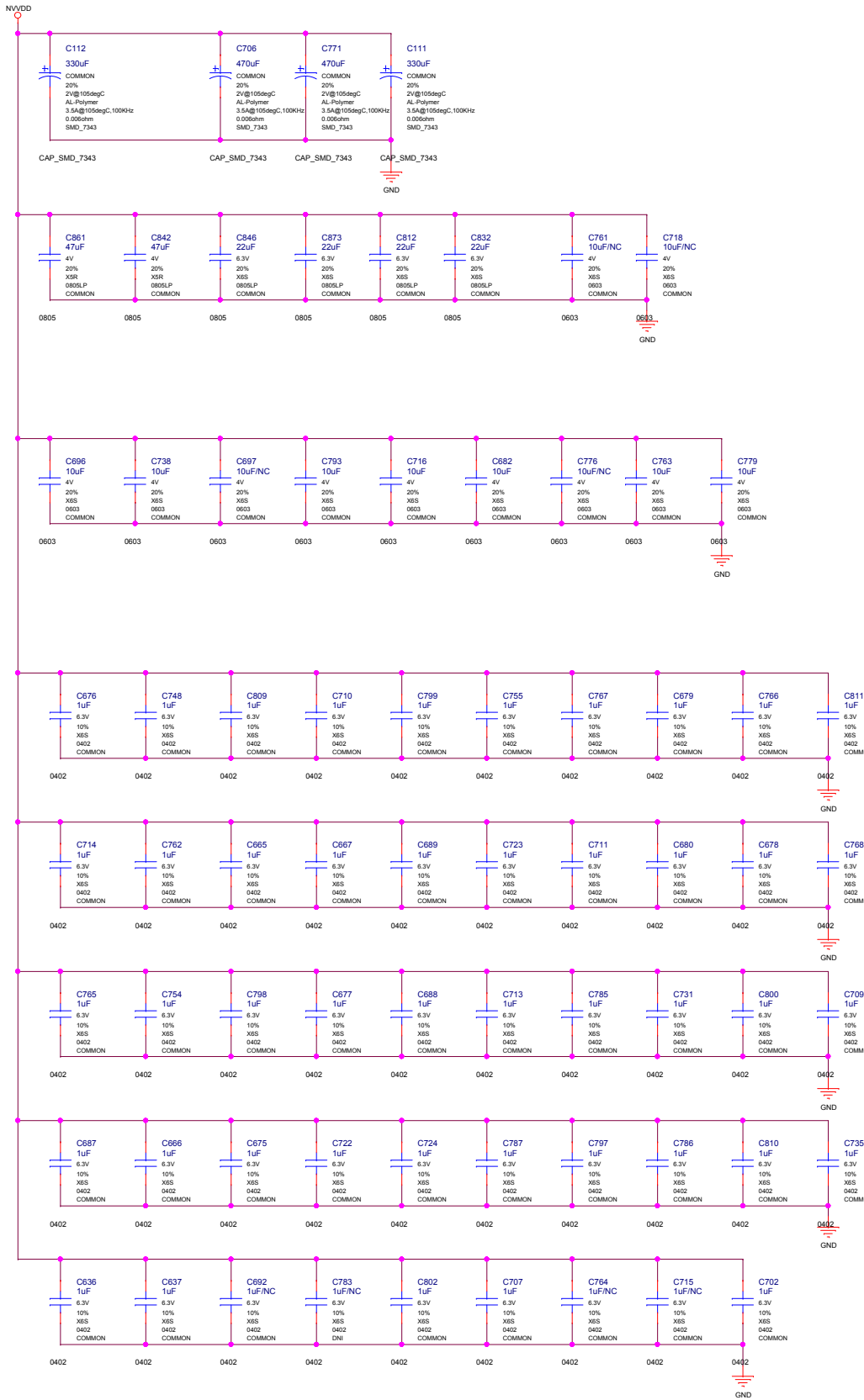
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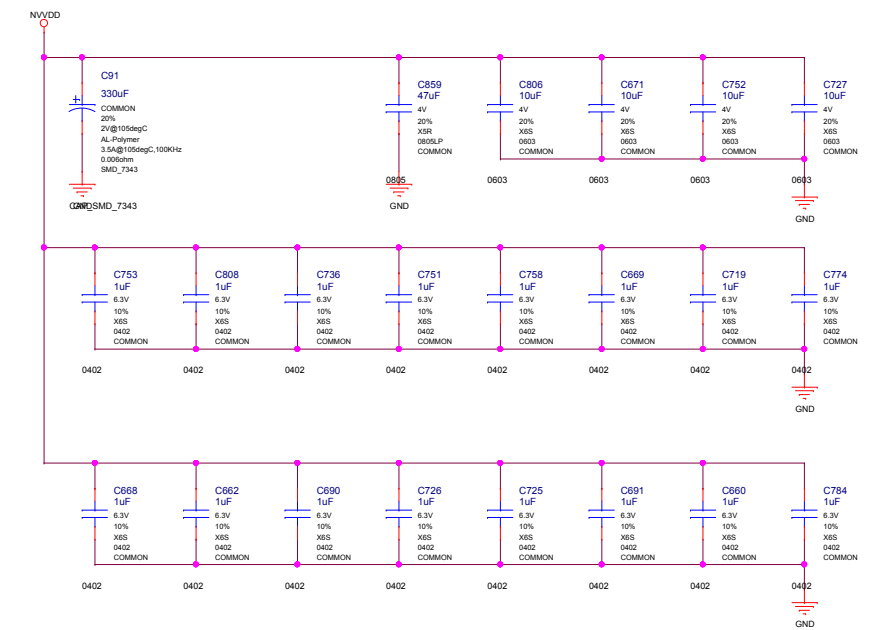
FBVDD



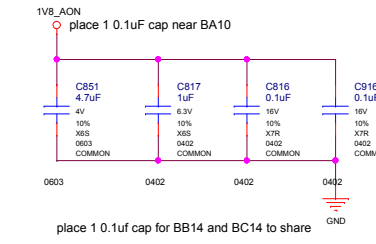
NVVD



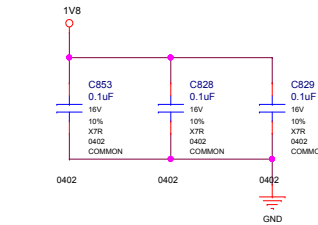
NVVD



1V8\_AON



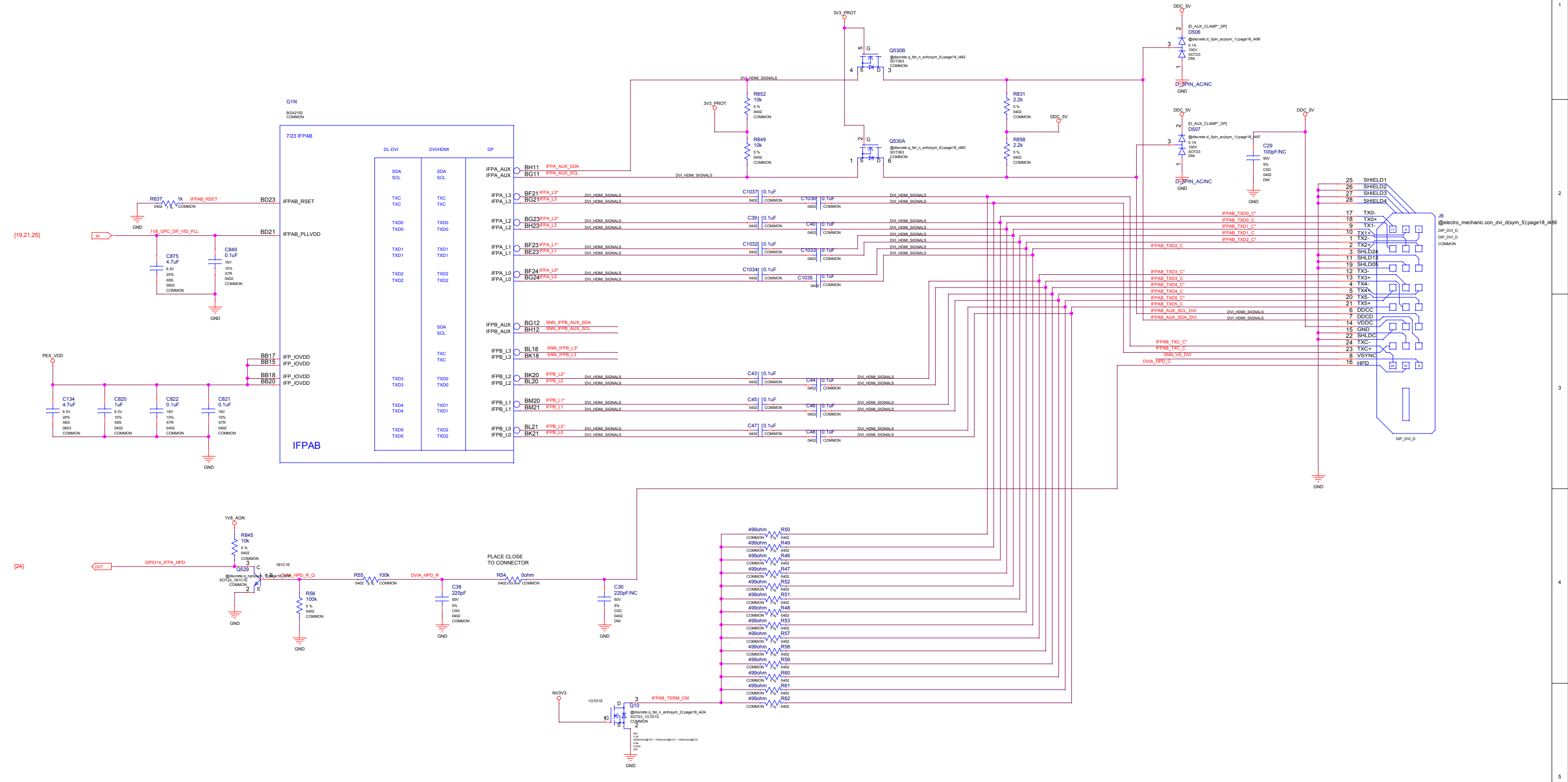
1V8\_MAIN



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ASSEMBLY PAGE DETAIL	-ASSEMBLY_DESCRIPTION- GPU Decoupling
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		Galaxy Microsystems (HK) Ltd.	
Page Name: GPU Decoupling			
Size: Custom	Project Name: P45U	Design By: Carson	Rev: V10
Date: Thursday, December 28, 2017	Sheet 17 of 37		
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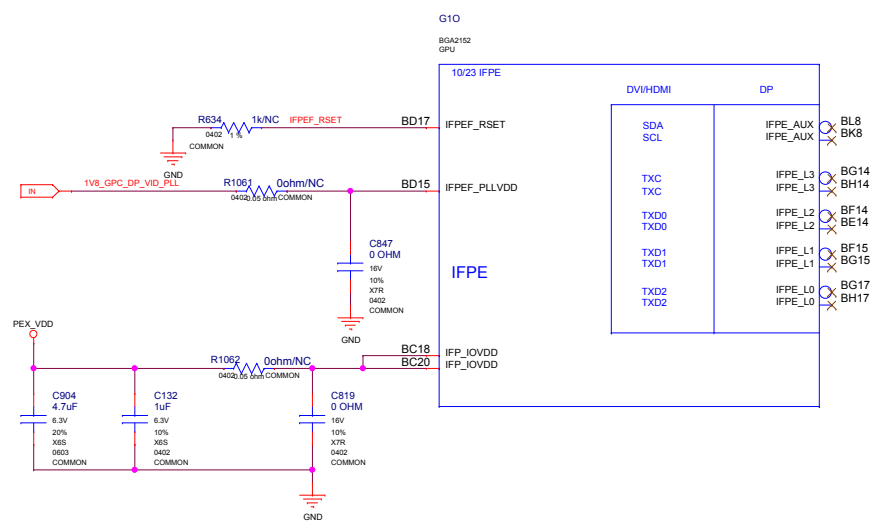
ASSEMBLY PAGE DETAIL	<ASSEMBLY_DESCRIPTION> IFPAB DVI-D-DL
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**GALAXY** Galaxy Microsystems (HK) Ltd.

Page Name: IFPAB DVI-D-DL

Size: Custom	Project Name: P45U	Design By: Carson	Rev: V10
Date: Thursday, December 28, 2017	Sheet: 18	of: 37	

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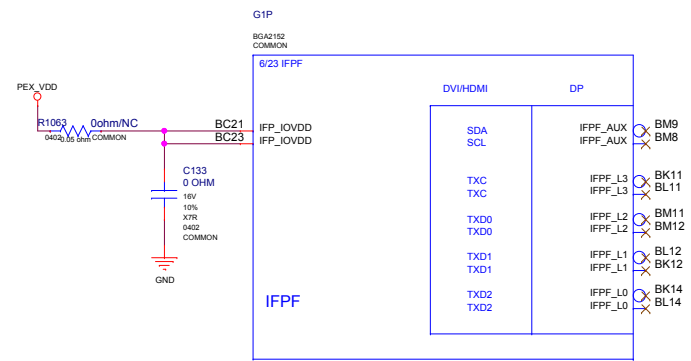
25)

5

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ASSEMBLY PAGE DETAIL	<ASSEMBLY_DESCRIPTION> IFPE DP
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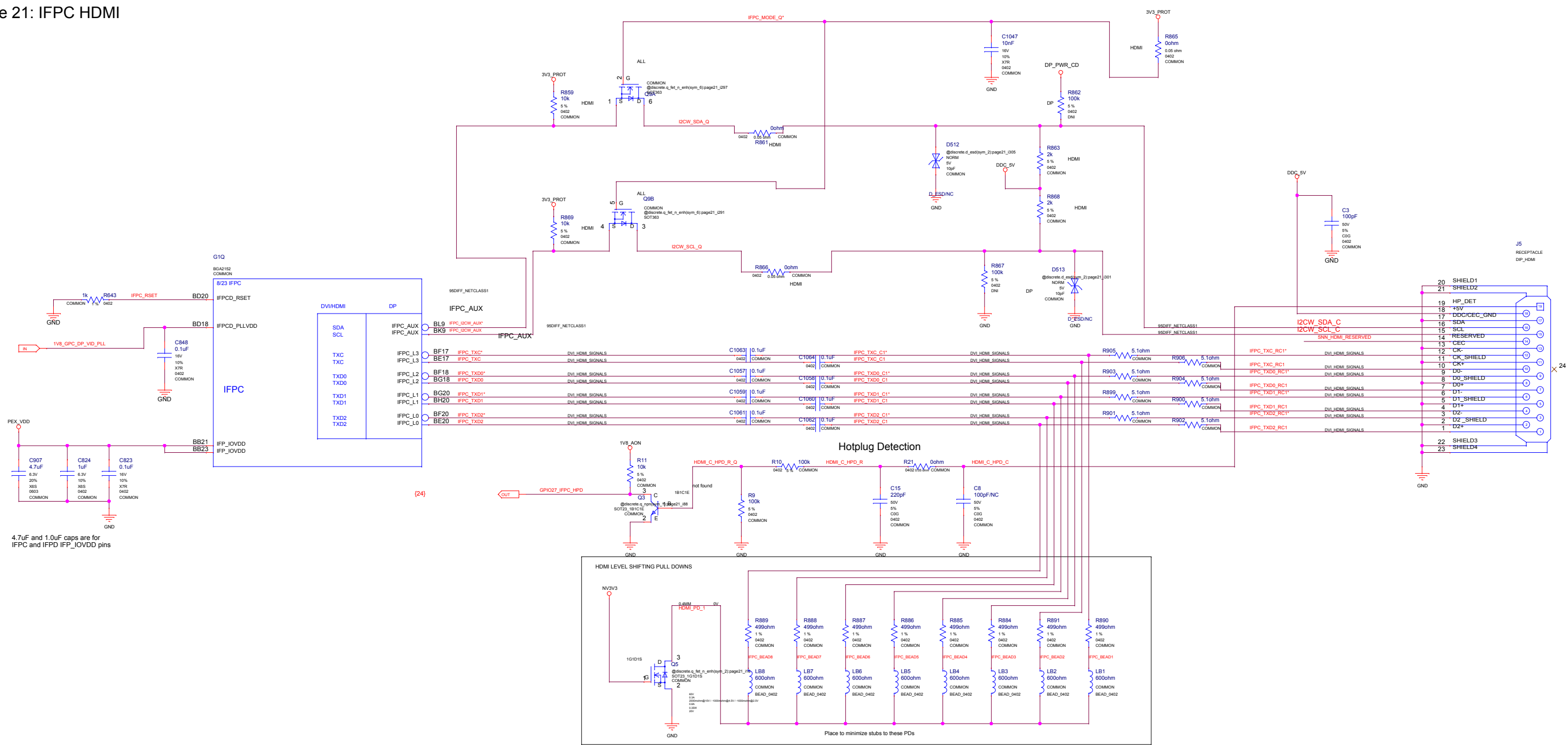
		Galaxy Microsystems (HK) Ltd.	
Page Name: IFPE UNUSED			
Size: Custom	Project Name: P45U	Design By: Carson	Rev: V10
Date: Thursday, December 28, 2017	Sheet 19 of 37		
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ASSEMBLY PAGE DETAIL	<ASSEMBLY_DESCRIPTION> IFPF DP
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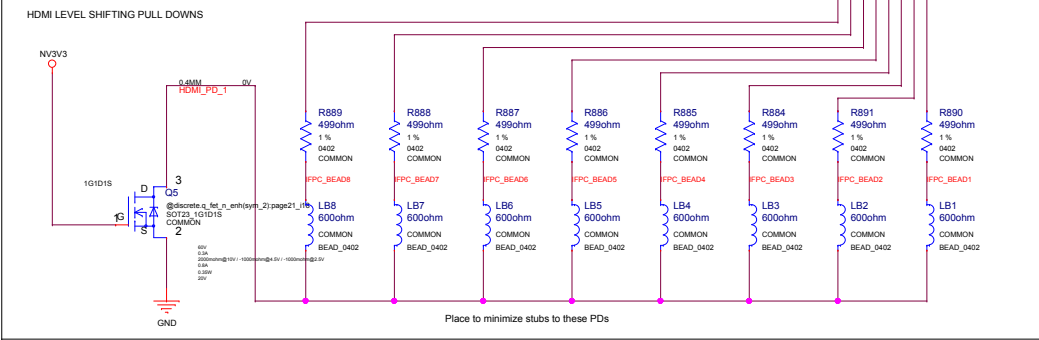
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Page Name: IFPF UNUSED			
Size: Custom	Project Name: P45U	Design By: Carson	Rev: V10
Date: Thursday, December 28, 2017	Sheet: 20	of	37
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4.7uF and 1.0uF caps are for IFPC and IFPD IFP\_IOVDD pins

(24)

Hotplug Detection



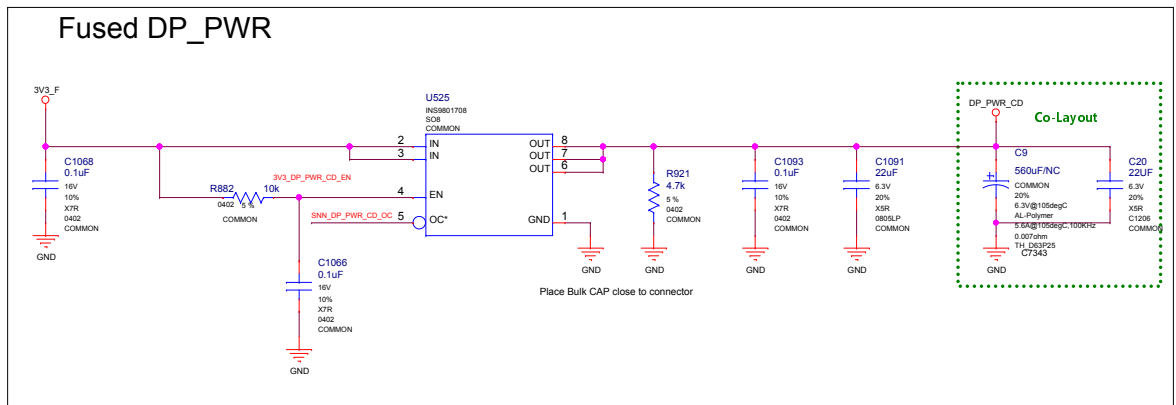
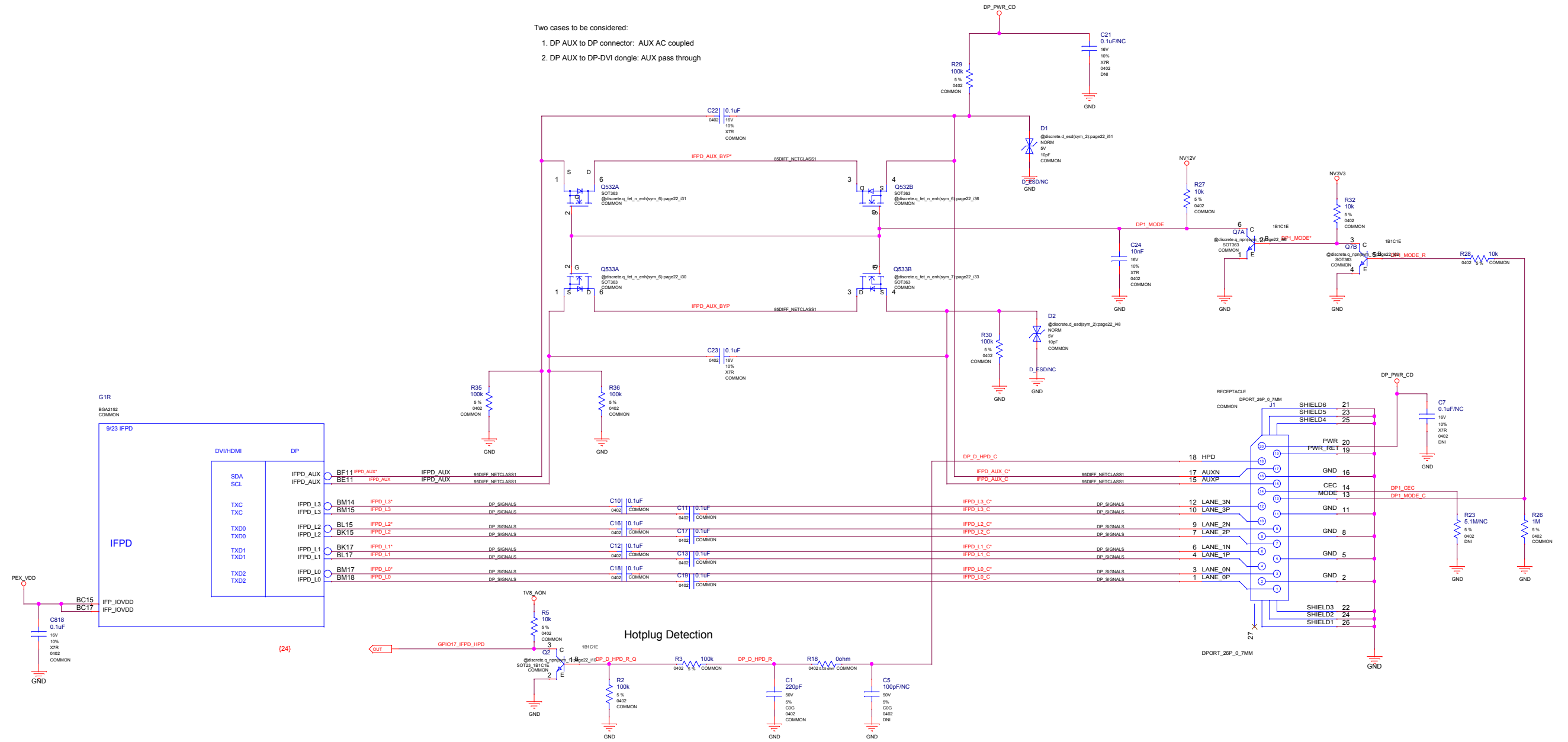
Place to minimize stubs to these PDs

		Galaxy Microsystems (HK) Ltd.	
Page Name: IFPC HDMI			
Size: Custom	Project Name: P45U	Design By: Carson	Rev: V10
Date: Thursday, December 28, 2017	Sheet: 21	of 37	
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ASSEMBLY PAGE DETAIL	<ASSEMBLY_DESCRIPTION> IFPC HDMI/DP
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Two cases to be considered:  
 1. DP AUX to DP connector: AUX AC coupled  
 2. DP AUX to DP-DVI dongle: AUX pass through



ASSEMBLY PAGE DETAIL	-ASSEMBLY_DESCRIPTION- IFPD DP
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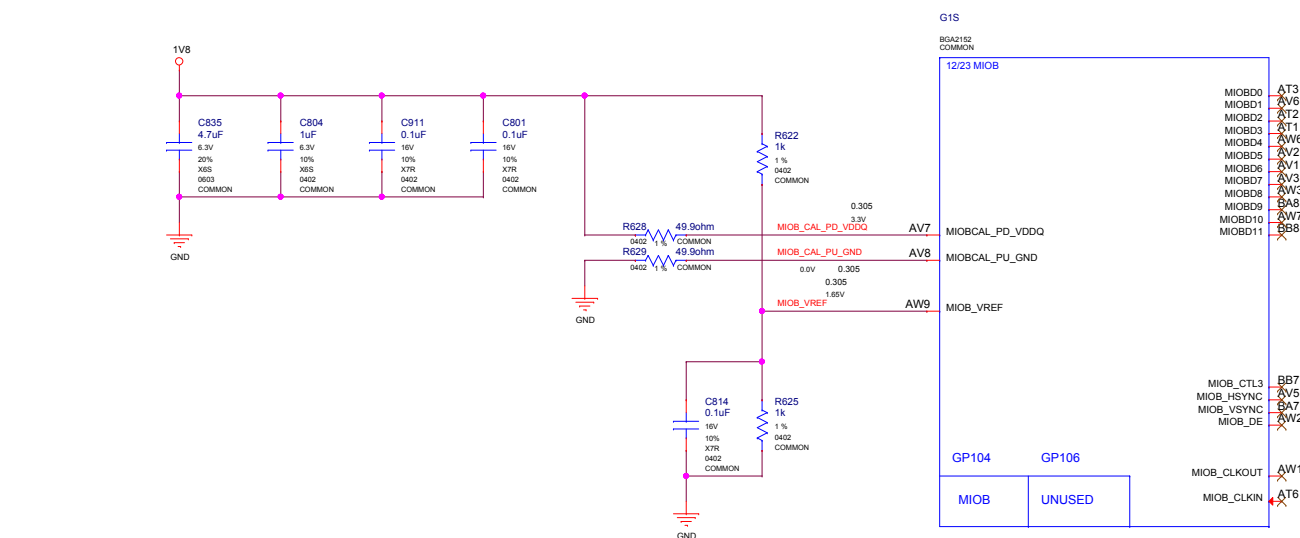
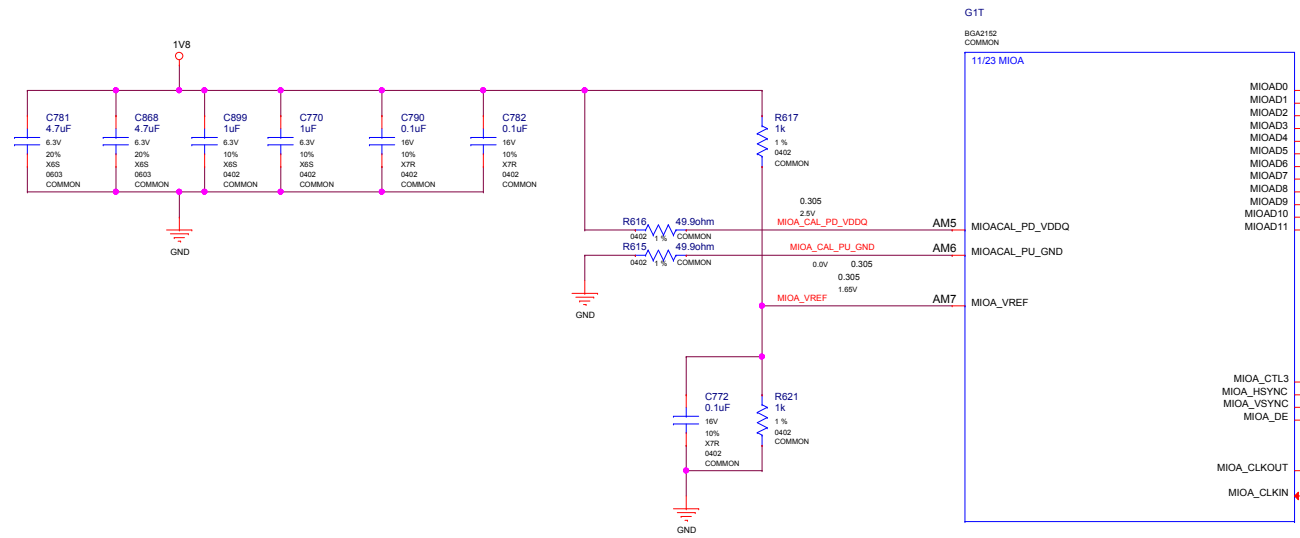
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Page Name: IFPD DP

Size: Custom	Project Name: P45U	Design By: Carson	Rev: V10
Date: Thursday, December 28, 2017	Sheet: 22	of 37	

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ASSEMBLY PAGE DETAIL	<ASSEMBLY_DESCRIPTION> MIOA/B Interface and Frame Lock
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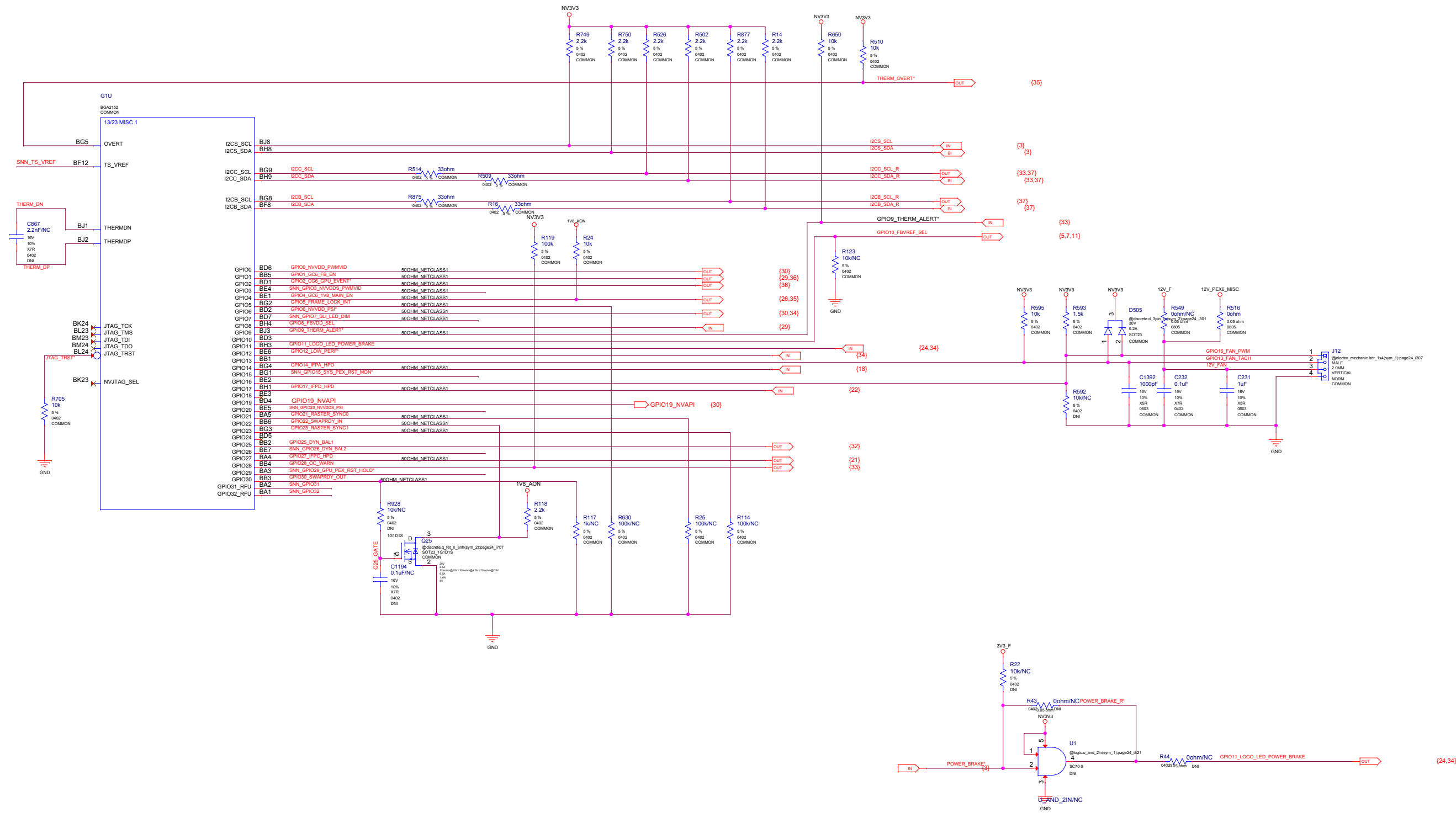
**GALAXY** Galaxy Microsystems (HK) Ltd.

Page Name: MIOA/B Interface and Frame Lock

Size: Custom	Project Name: P45U	Design By: Carson	Rev: V10
Date: Thursday, December 28, 2017	Sheet: 23	of: 37	

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ASSEMBLY PAGE DETAIL	<ASSEMBLY_DESCRIPTION> MISC1: Fan, Thermal, JTAG, GPIO, STEREO
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**GALAXY** Galaxy Microsystems (HK) Ltd.

Page Name: MISC1: Fan, Thermal, JTAG, GPIO, STEREO

Size: Custom	Project Name: P45U	Design By: Carson	Rev: V10
Date: Thursday, December 28, 2017	Sheet: 24	of: 37	

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STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

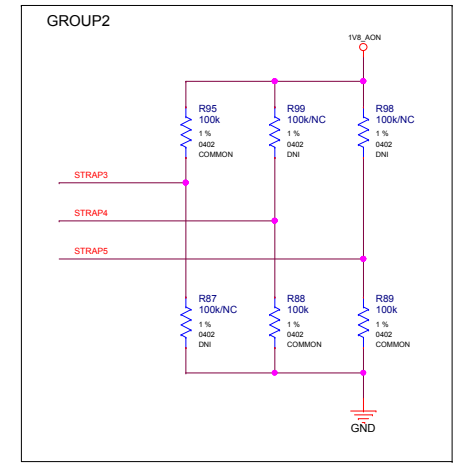
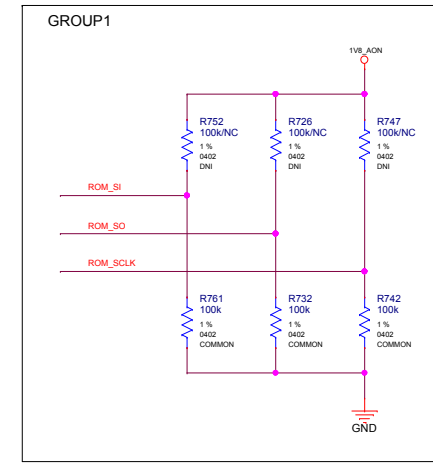
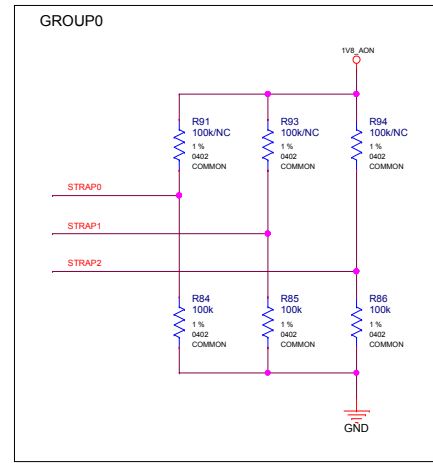
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	L	L	0110	
L	M	L	0101	
L	M	H	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	0	0
L	M	L	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

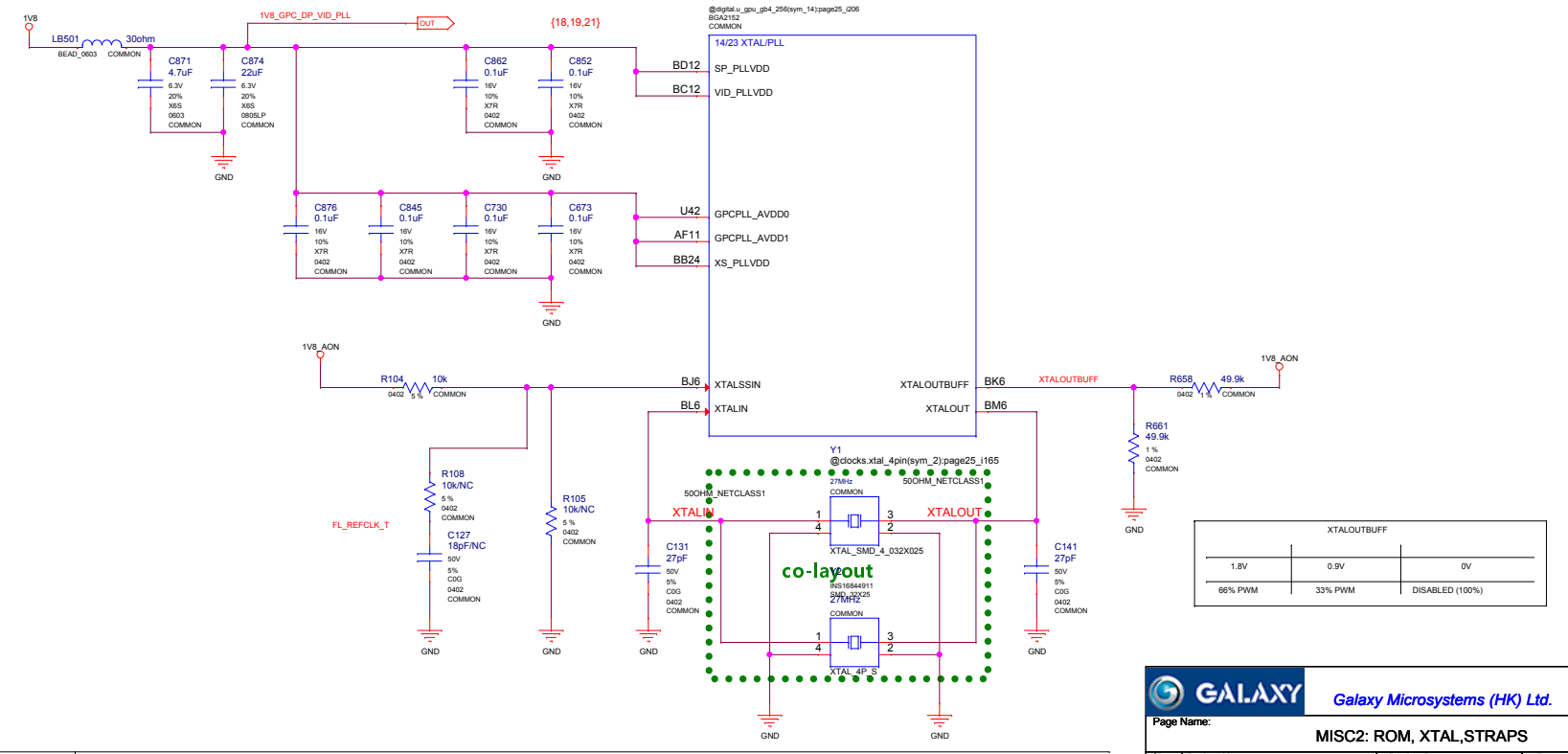
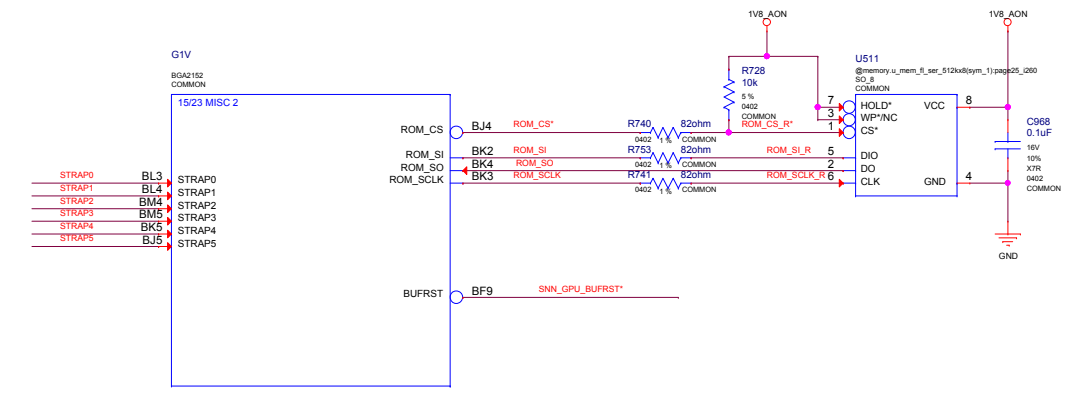
H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE  
1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL  
1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER  
1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE

ASSEMBLY PAGE DETAIL <ASSEMBLY\_DESCRIPTION> MISC2: ROM, XTAL,STRAPS



CFG[3:0]	Config	Width	Vendor
0000	256Mx32	256-bit	Samsung
0001	256Mx32	256-bit	Micron
0010	256Mx32	256-bit	Hynix
0011	Reserved		
0100	Reserved		
0101	Reserved		
0110	Reserved		
0111	Reserved		



XTALOUTBUFF		
1.8V	0.9V	0V
66% PWM	33% PWM	DISABLED (100%)

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Page Name: MISC2: ROM, XTAL,STRAPS

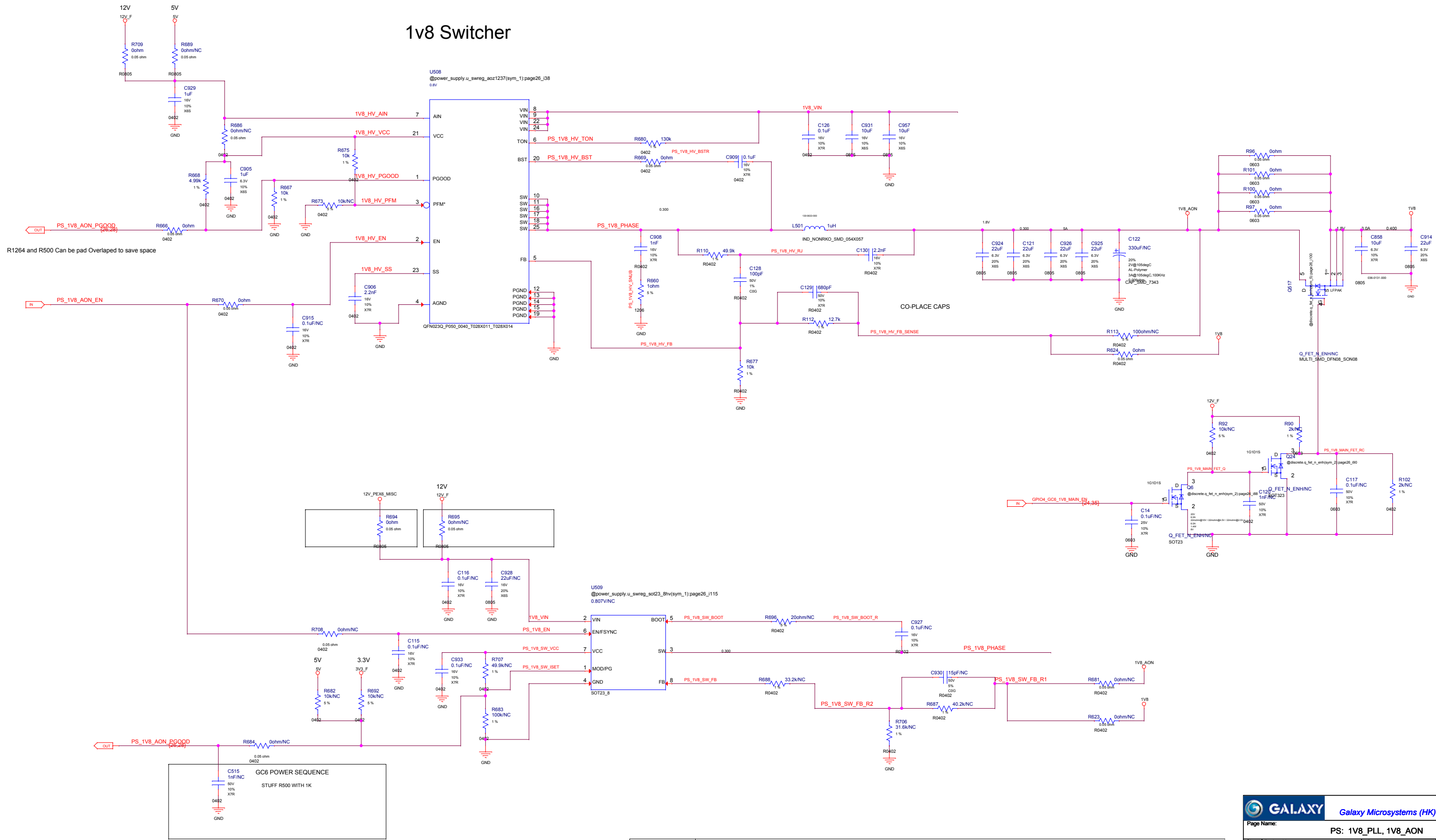
Size: Custom Project Name: P45U Design By: Carson Rev: V10

Date: Thursday, December 28, 2017 Sheet: 25 of 37

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# 1v8 Switcher



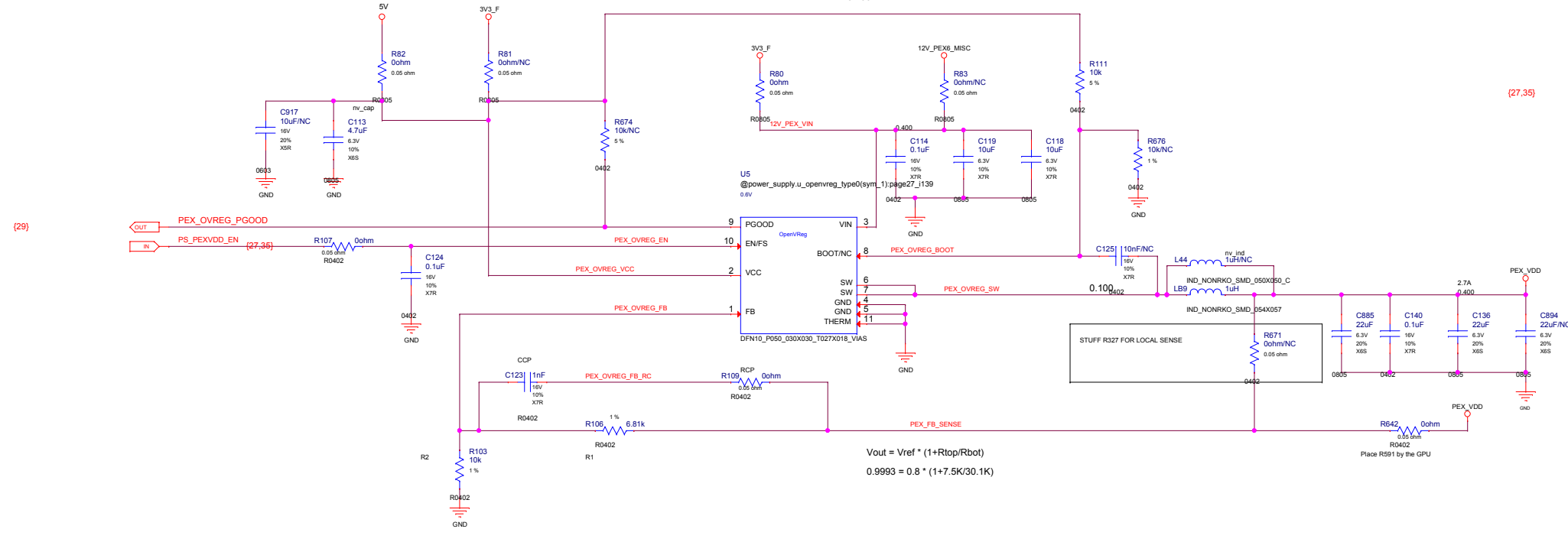
28,29,35

ASSEMBLY PAGE DETAIL	<ASSEMBLY_DESCRIPTION> PS: 1V8_PLL, 1V8_AON
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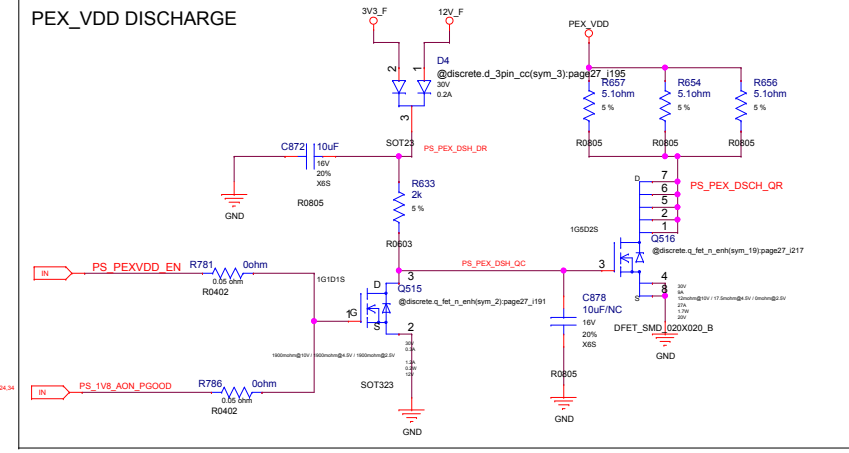
<b>GALAXY</b> Galaxy Microsystems (HK) Ltd.			
Page Name: PS: 1V8_PLL, 1V8_AON			
Size: Custom	Project Name: P45U	Design By: Carson	Rev: V10
Date: Thursday, December 28, 2017	Sheet: 26	of 37	
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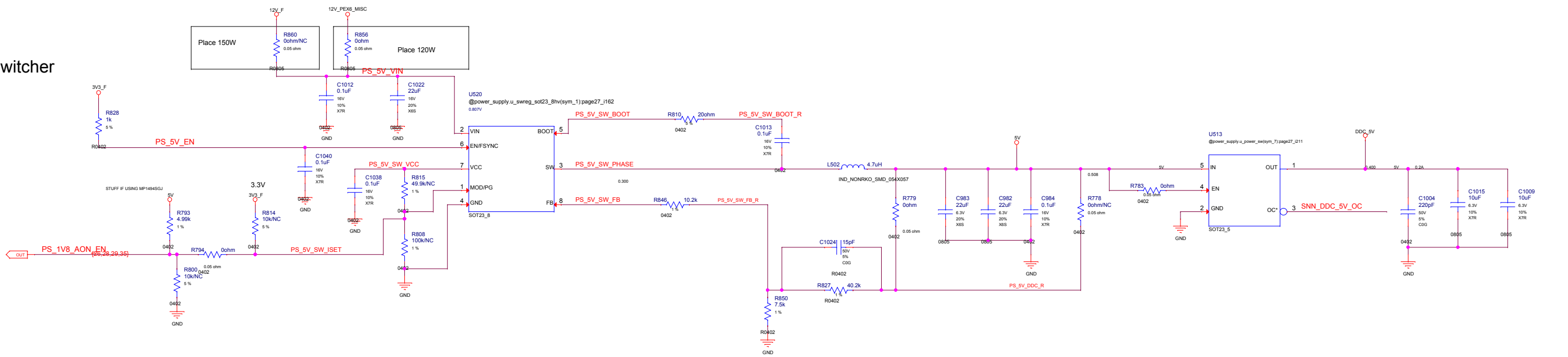
PEX PLL Switcher



PEX\_VDD DISCHARGE



5V Switcher



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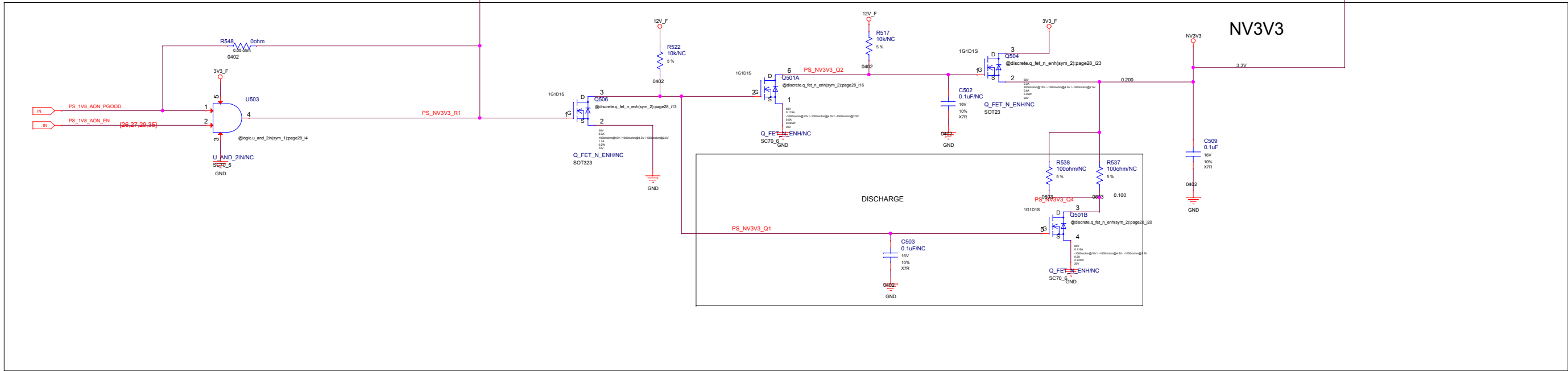
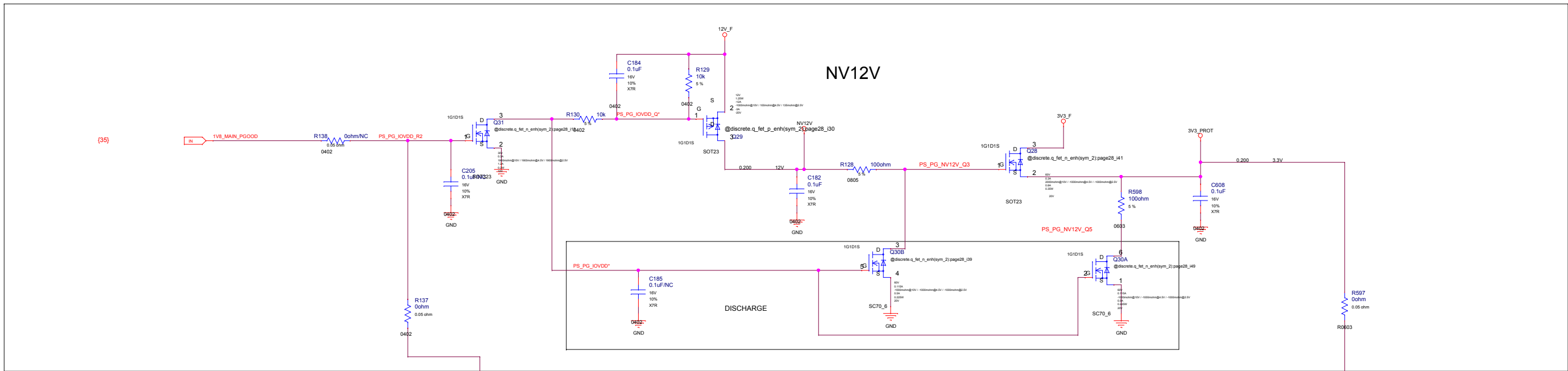
ASSEMBLY PAGE DETAIL	<ASSEMBLY_DESCRIPTION> PS: 5V, PEX_VDD
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**GALAXY** Galaxy Microsystems (HK) Ltd.

Page Name: PS: 5V, PEX\_VDD

Size: Custom	Project Name: P45U	Design By: Carson	Rev: V10
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ASSEMBLY PAGE DETAIL	<ASSEMBLY_DESCRIPTION> PS: NV3V3, NV12V
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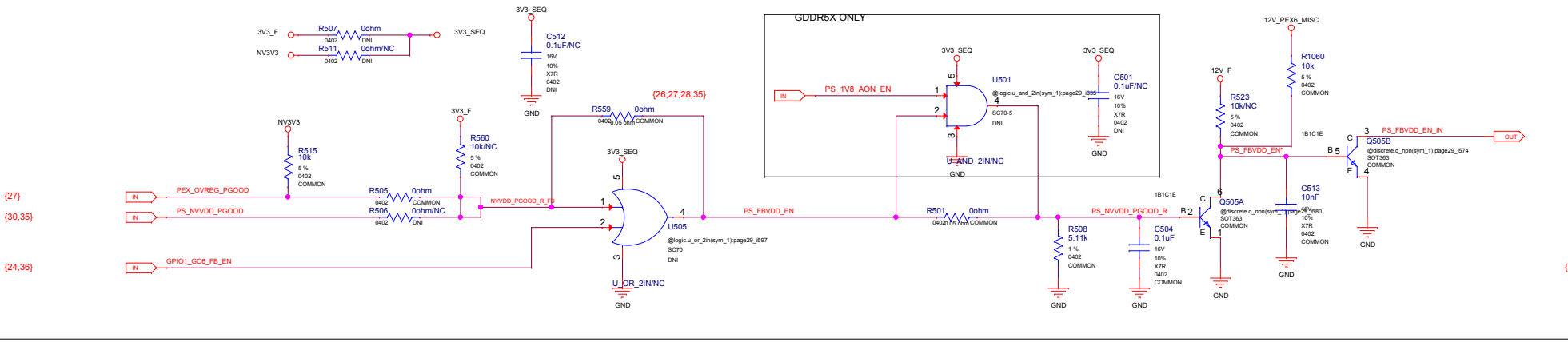
Page Name: PS: NV3V3, NV12V

Size: Custom	Project Name: P45U	Design By: Carson	Rev: V10
Date: Thursday, December 28, 2017	Sheet: 28	of: 37	

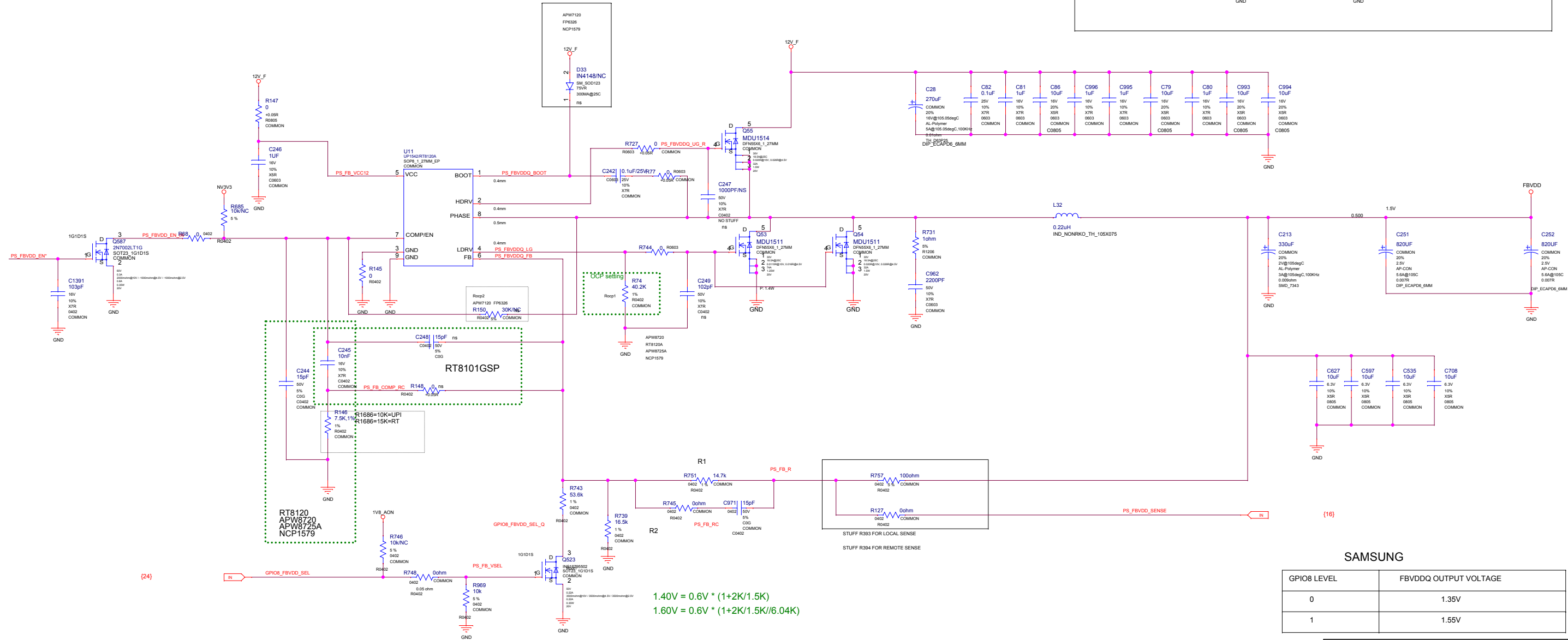
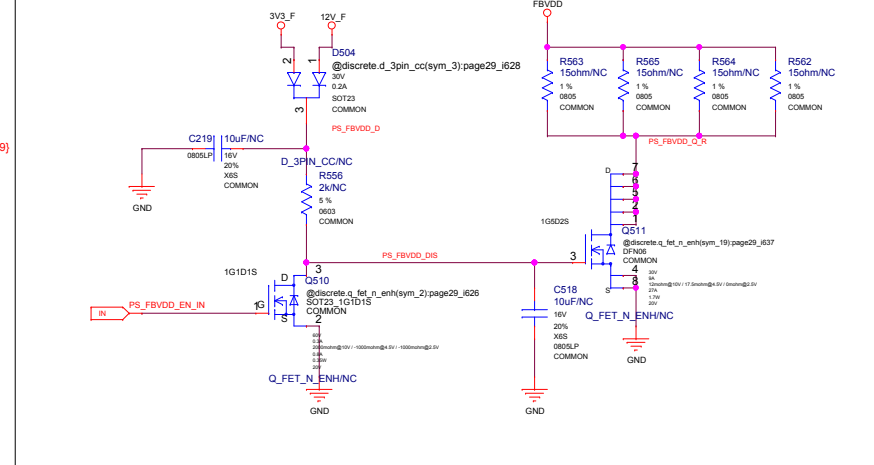
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FBVDD	NETNAME	MAX_CURRENT	MIN_LINE_WIDTH	VOLTAGE
-------	---------	-------------	----------------	---------

FBVDD/Q Enable



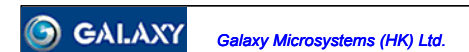
FBVDD DISCHARGE



$1.40V = 0.6V * (1+2K/1.5K)$   
 $1.60V = 0.6V * (1+2K/1.5K/6.04K)$

SAMSUNG

GPIO8 LEVEL	FBVDDQ OUTPUT VOLTAGE
0	1.35V
1	1.55V

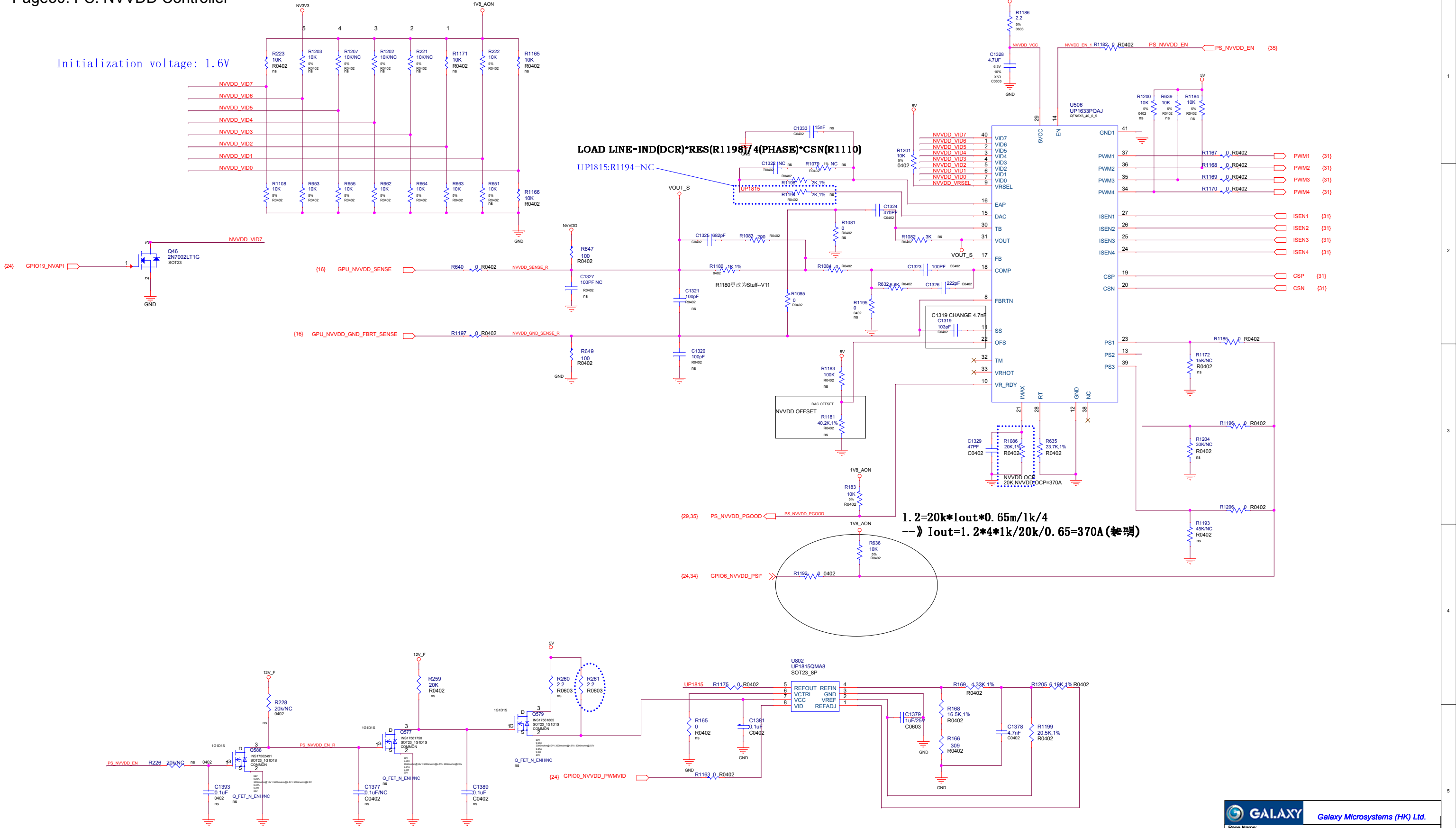


Page Name:	PS: FBVDD		
Size:	Project Name: P45U	Design By: Carson	Rev: V10
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ASSEMBLY PAGE DETAIL	-ASSEMBLY DESCRIPTION- PS: FBVDD
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Initialization voltage: 1.6V



LOAD LINE=IND(DCR)\*RES(R1198)/4(PHASE)\*CSN(R1110)

UPI815:R1194=NC

1.2=20k\*Iout\*0.65m/1k/4

--> Iout=1.2\*4\*1k/20k/0.65=370A (满载)

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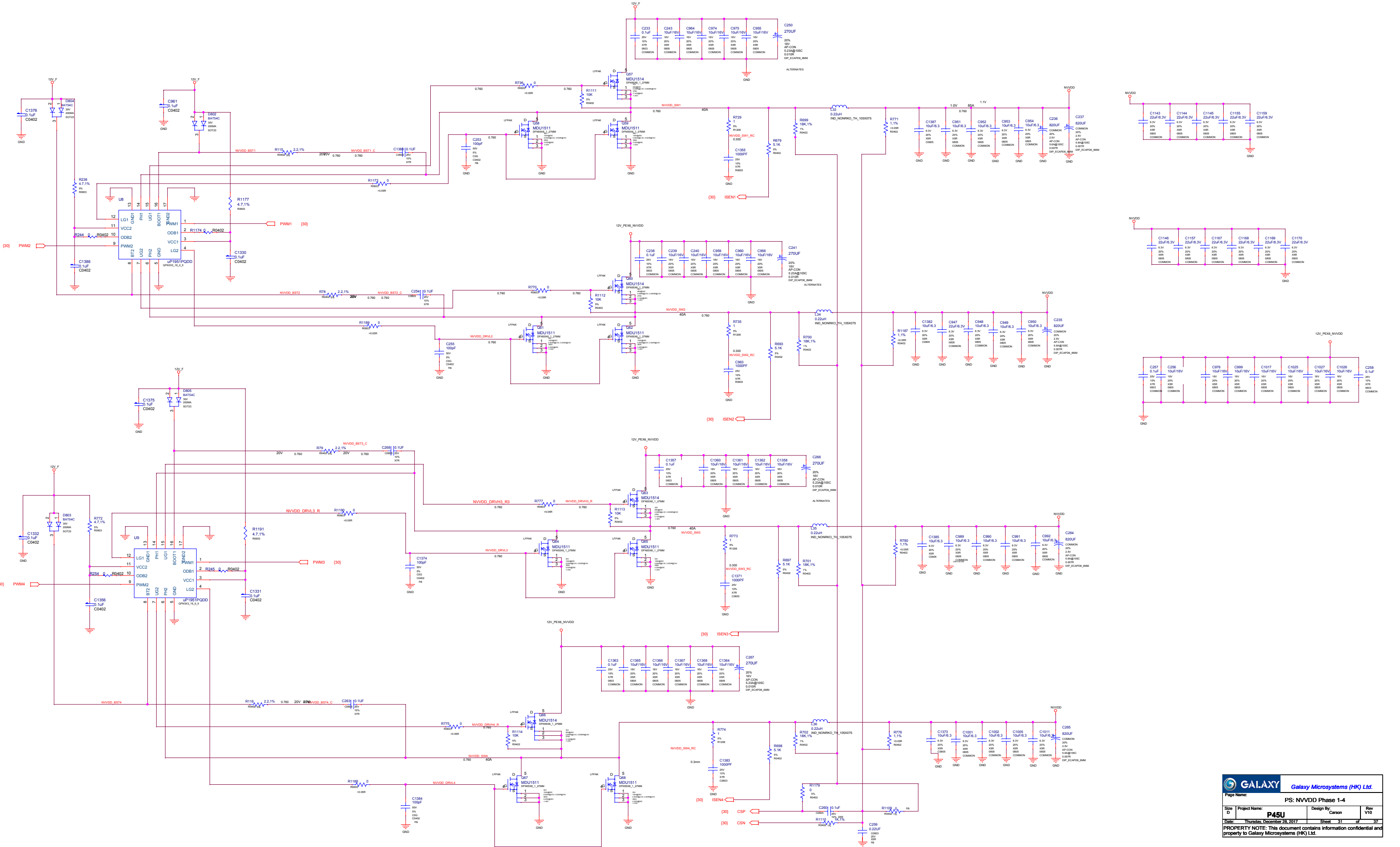
**GALAXY** Galaxy Microsystems (HK) Ltd.

Page Name: PS: NVVDD Controller

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Date: Thursday, December 28, 2017	Sheet: 30	of: 37	

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ASSEMBLY PAGE DETAIL	<ASSEMBLY_DESCRIPTION> PS: NVVDD Controller
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**GALAXY** Galaxy Microsystems (HK) Ltd.

Page Name: PS: NVDD Phase 1-4

Size D	Project Name: P45U	Design By: Carson	Rev: V10
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A B C D E F G H

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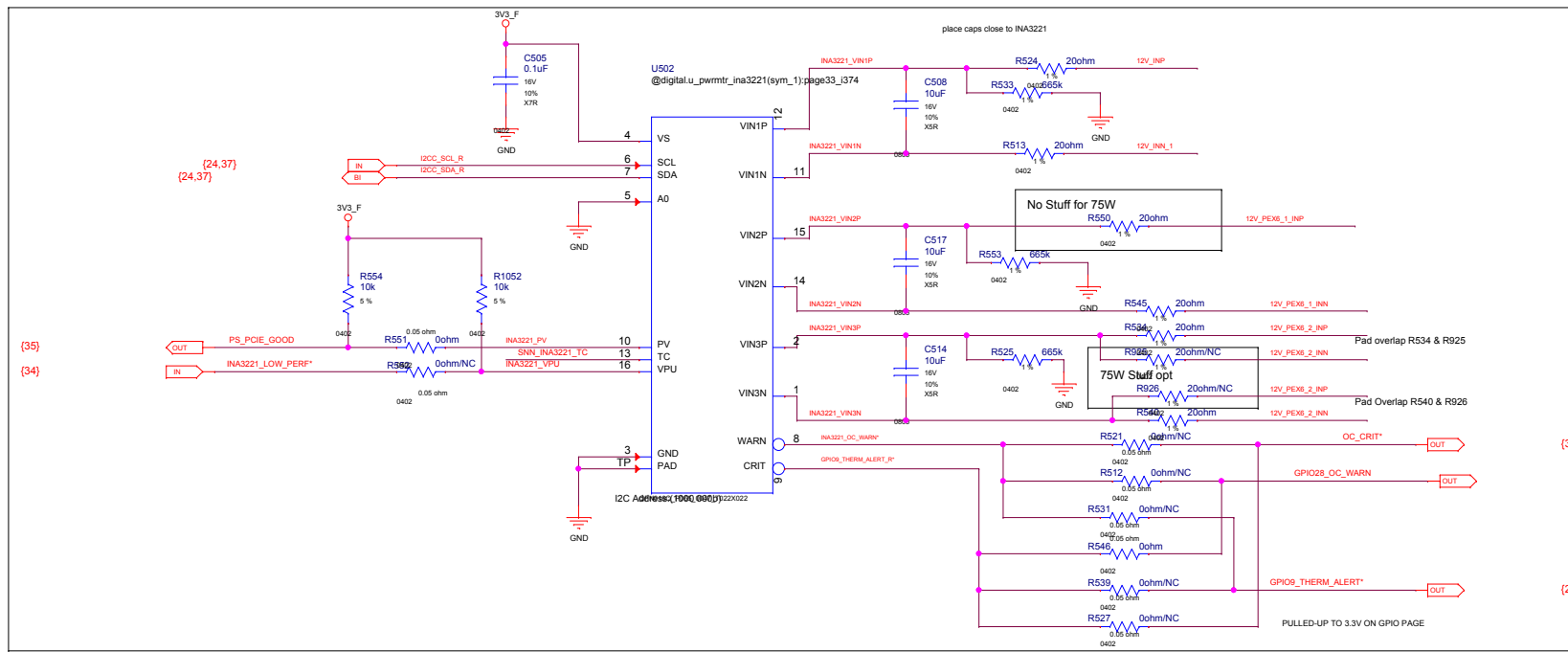
		Galaxy Microsystems (HK) Ltd.	
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Size: Custom	Project Name: <b>P45U</b>	Design By: Carson	Rev: V10
Date: Thursday, December 28, 2017	Sheet 32	of	37
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ASSEMBLY PAGE DETAIL	-ASSEMBLY_DESCRIPTION- PS: NVVDD Rail Balance Login & Dynamic Phase
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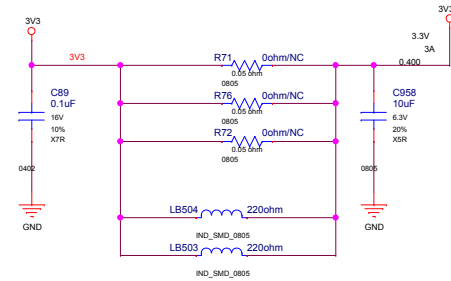
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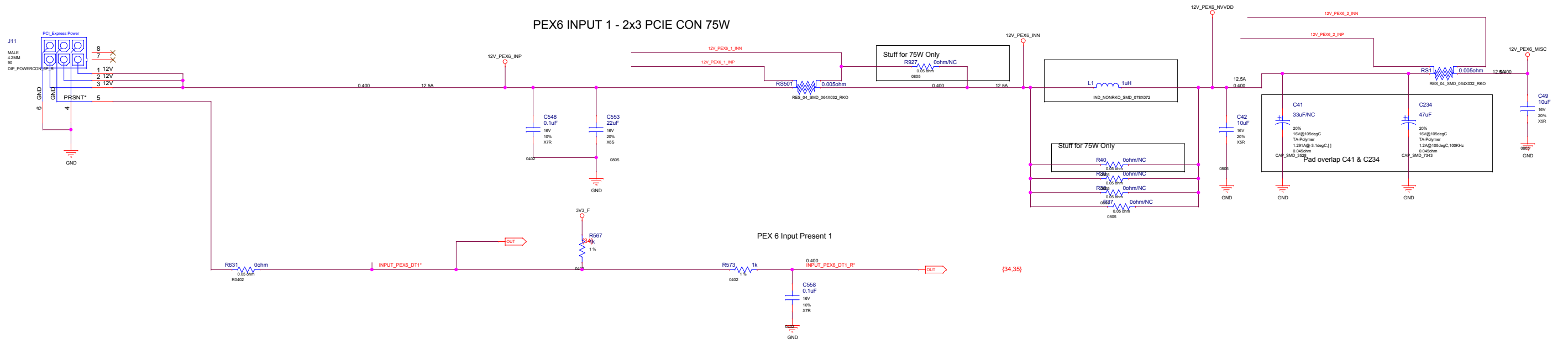




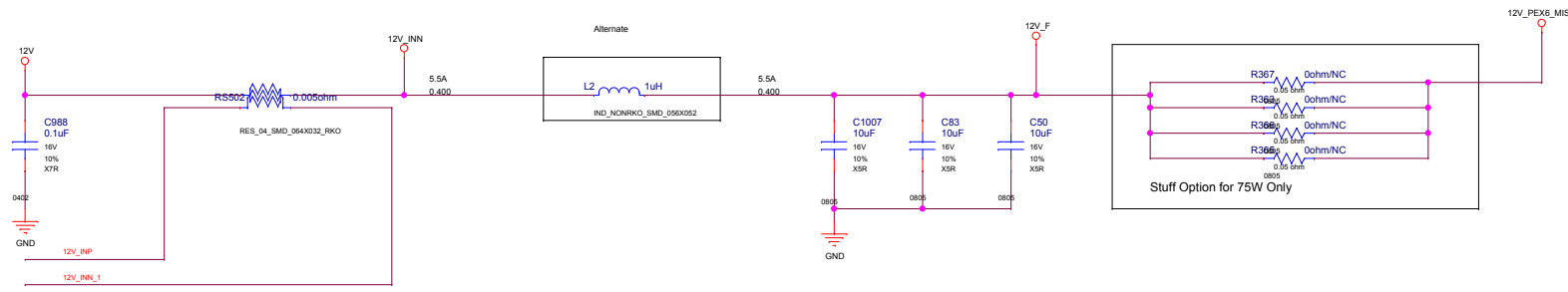
PEX 3V3 INPUT - 10W



PEX6 INPUT 1 - 2x3 PCIE CON 75W



PEX\_12V INPUT - 66W



Place close to J14/J16  
 J14 and J16 is the soldering holes for power cable.  
 The power cable Need a separate wire as detect pin  
 This detect wire need be soldered on J15

ASSEMBLY PAGE DETAIL	ASSEMBLY DESCRIPTION PS: Input, Filtering, and Monitoring
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**GALAXY** Galaxy Microsystems (HK) Ltd.

Page Name: PS: Input, Filtering, and Monitoring

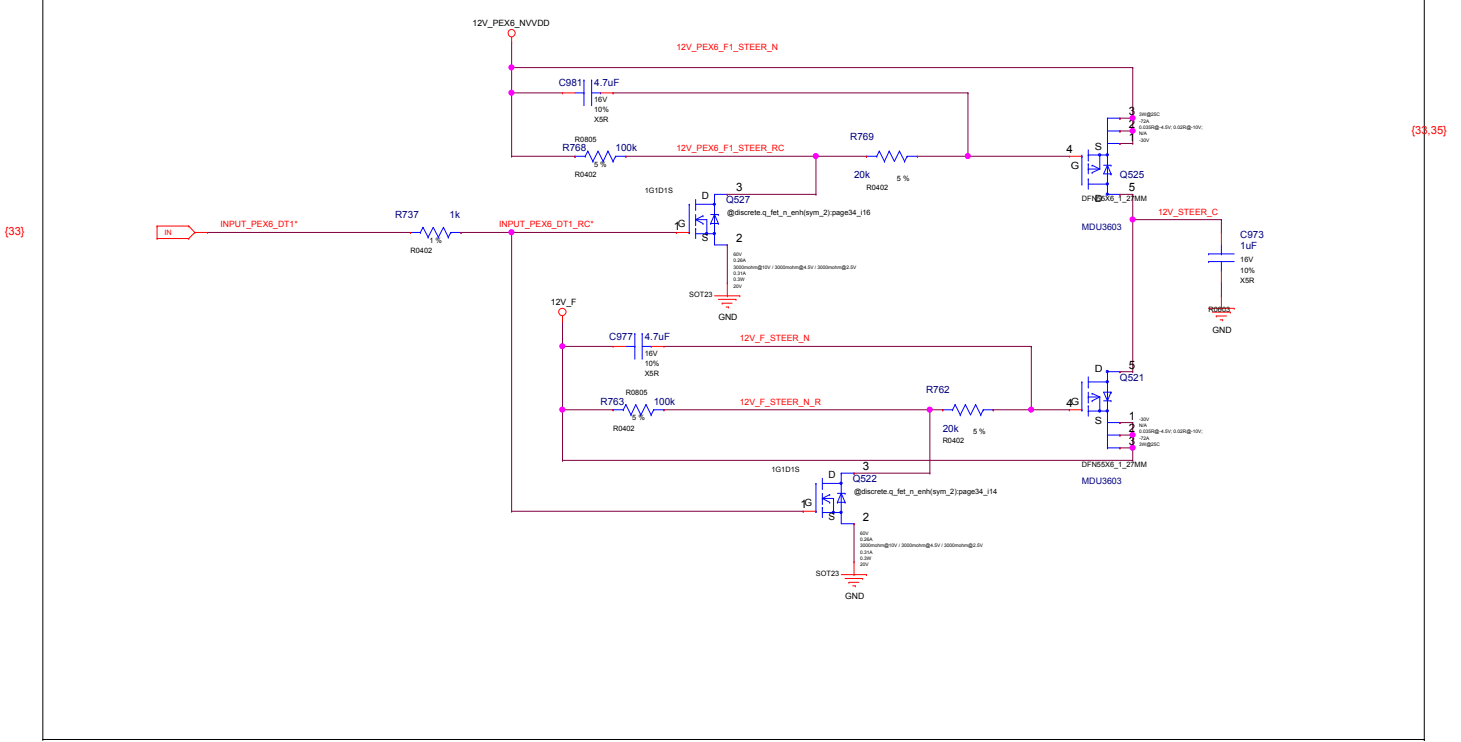
Size: Custom	Project Name: P45U	Design By: Carson	Rev: V10
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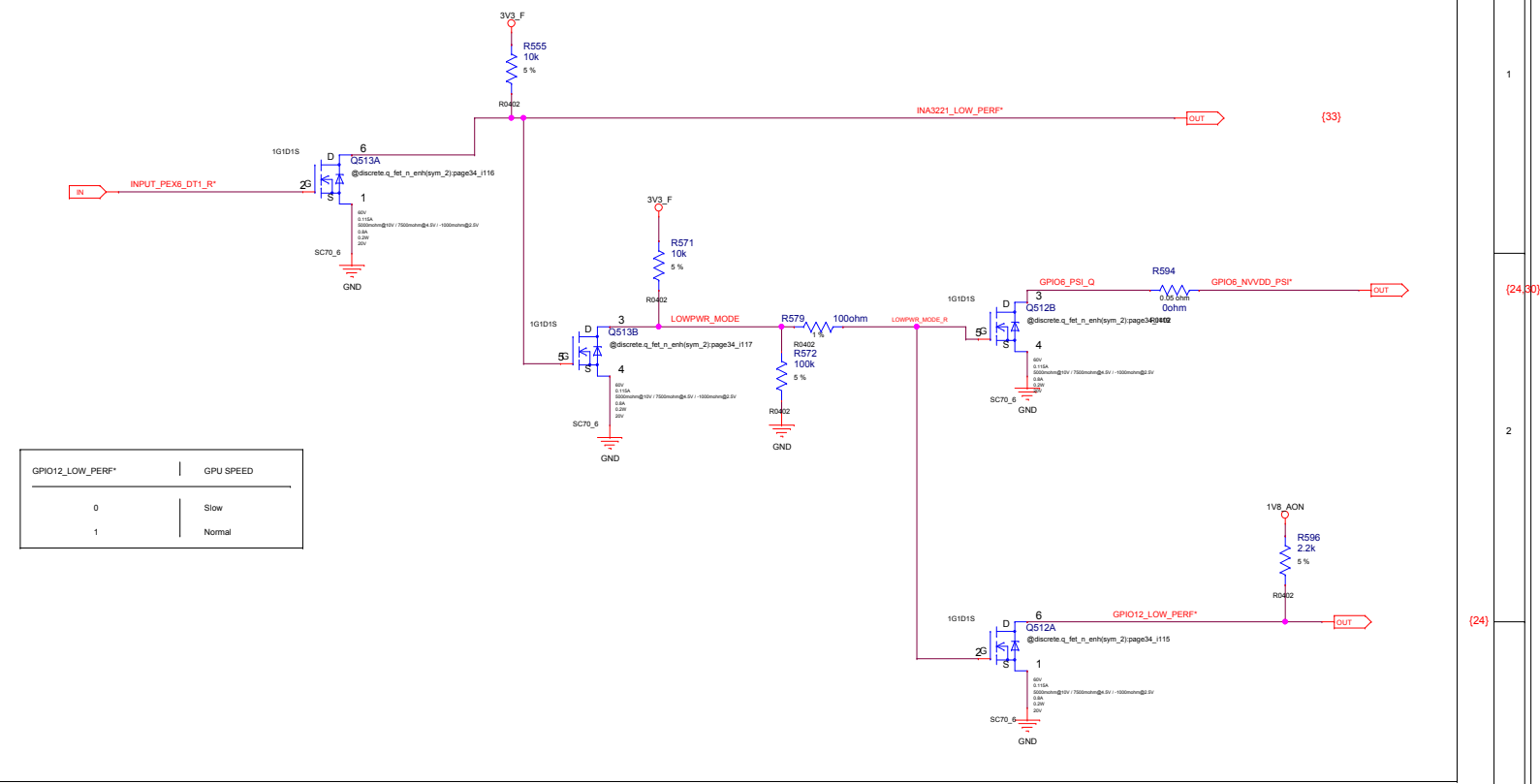
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12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA

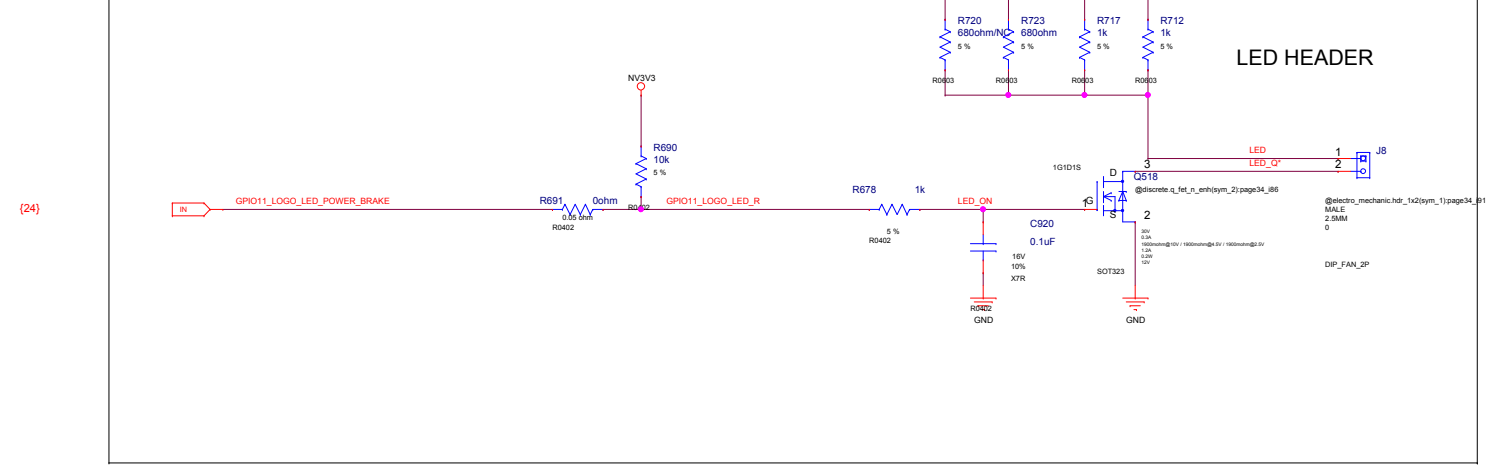


PEX Input - Power Level/PSI\* Control



GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

GeForce Logo LED



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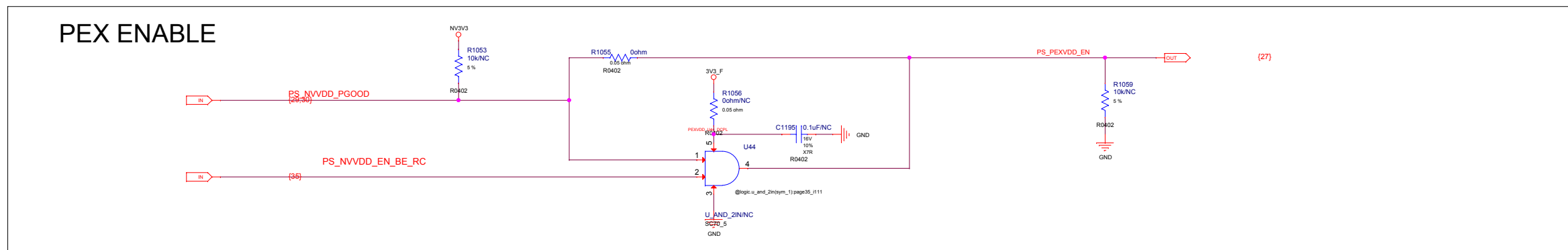
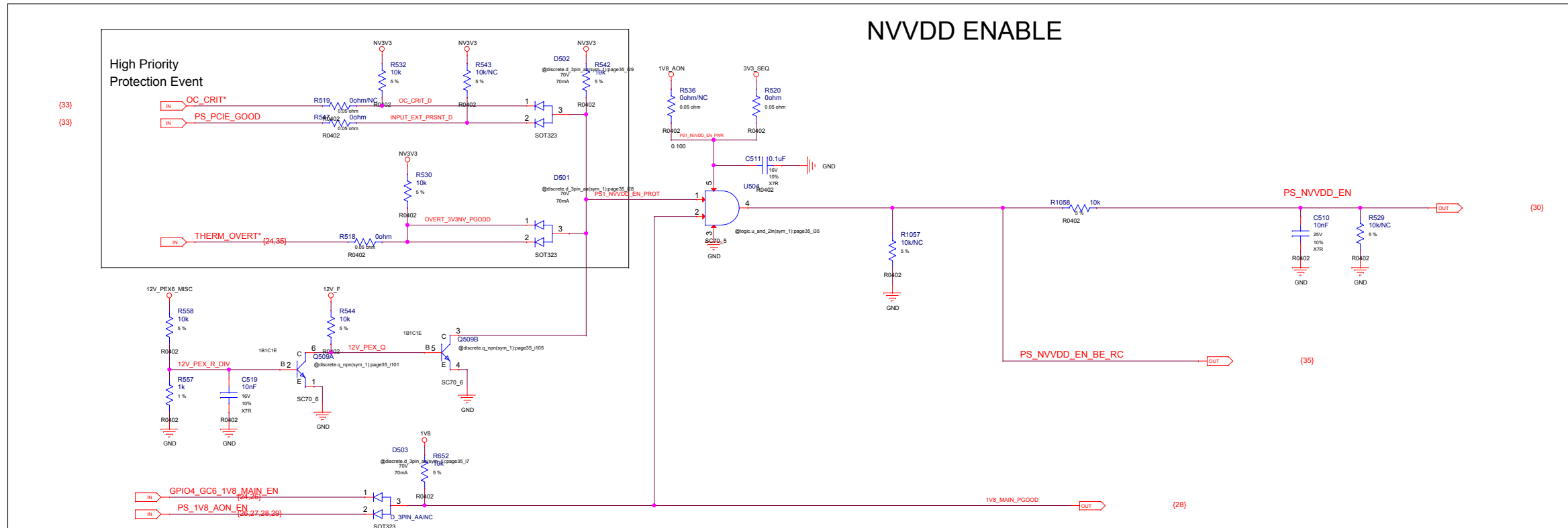
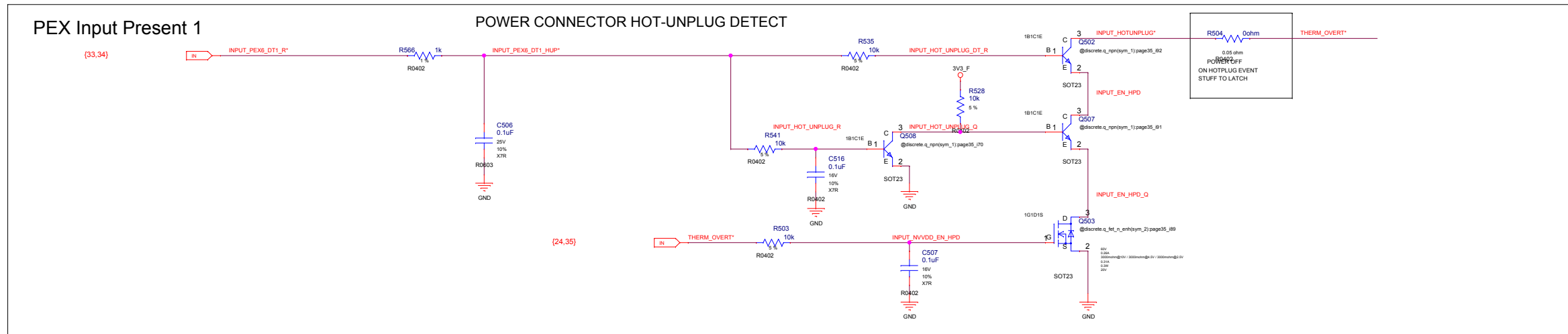
ASSEMBLY PAGE DETAIL	ASSEMBLY DESCRIPTION
	PS: 12V Power Steering, PSI Control & LED

**GALAXY** Galaxy Microsystems (HK) Ltd.

Page Name: PS: 12V Power Steering, PSI Control & LED

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ASSEMBLY PAGE DETAIL	<ASSEMBLY_DESCRIPTION> PS: Shut Down and Sequencing
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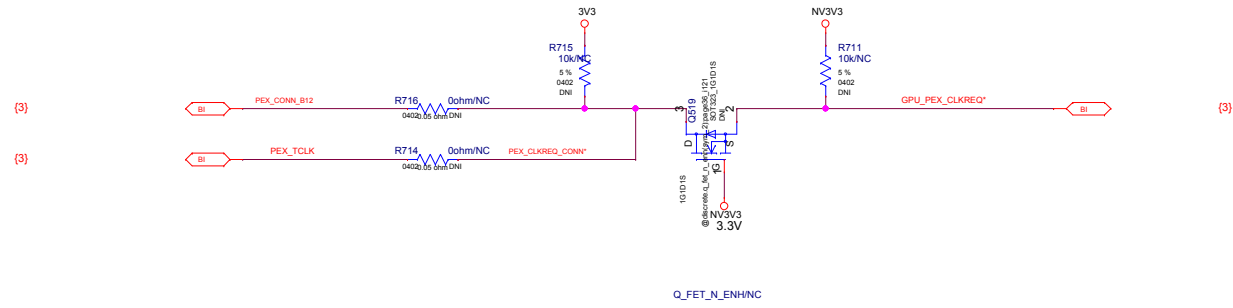
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Page Name: PS: Shut Down and Sequencing

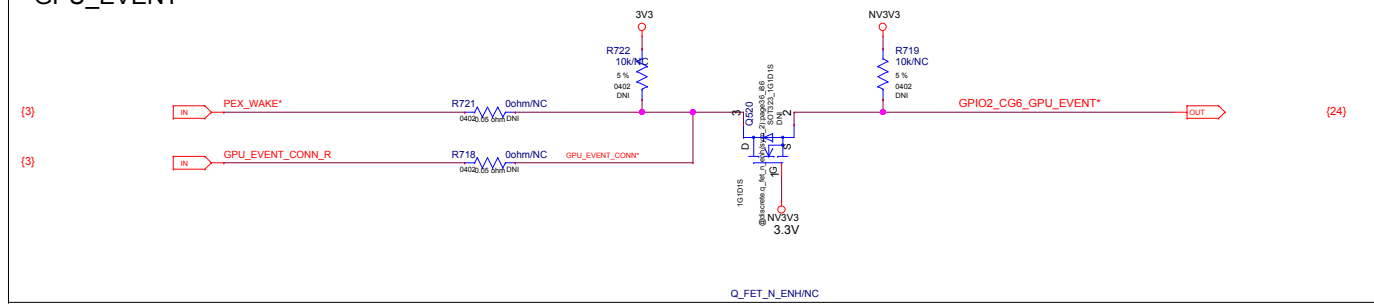
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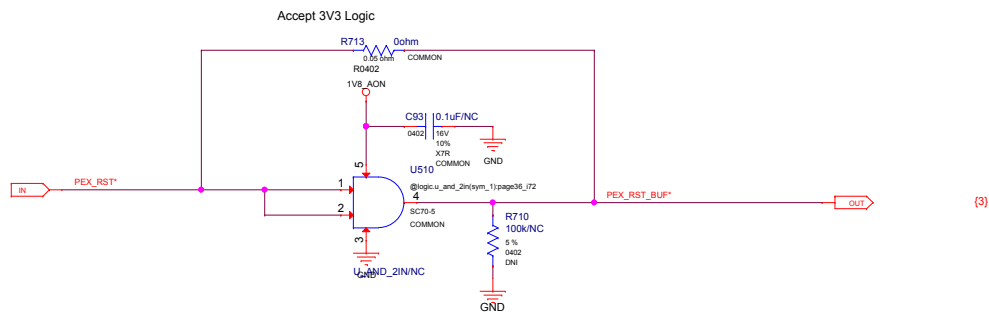
PEX\_CLKREQ\*



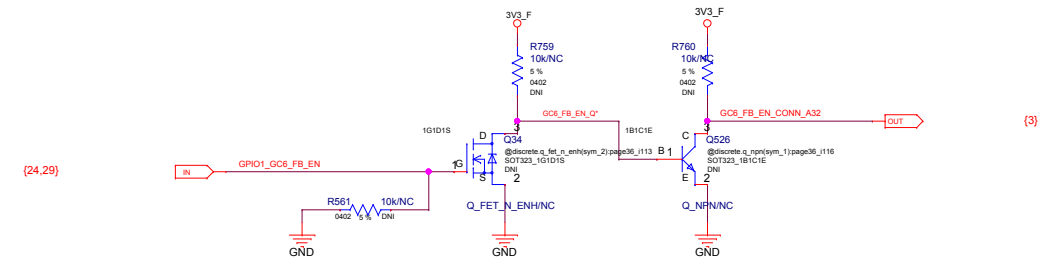
GPU\_EVENT\*



PEX\_RST# LOGIC



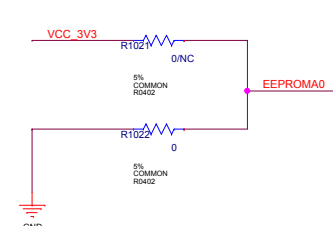
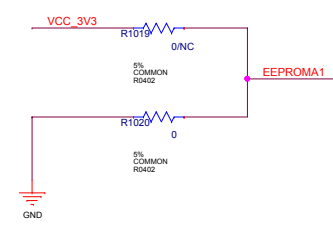
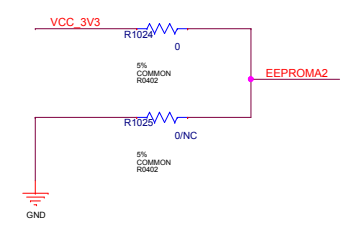
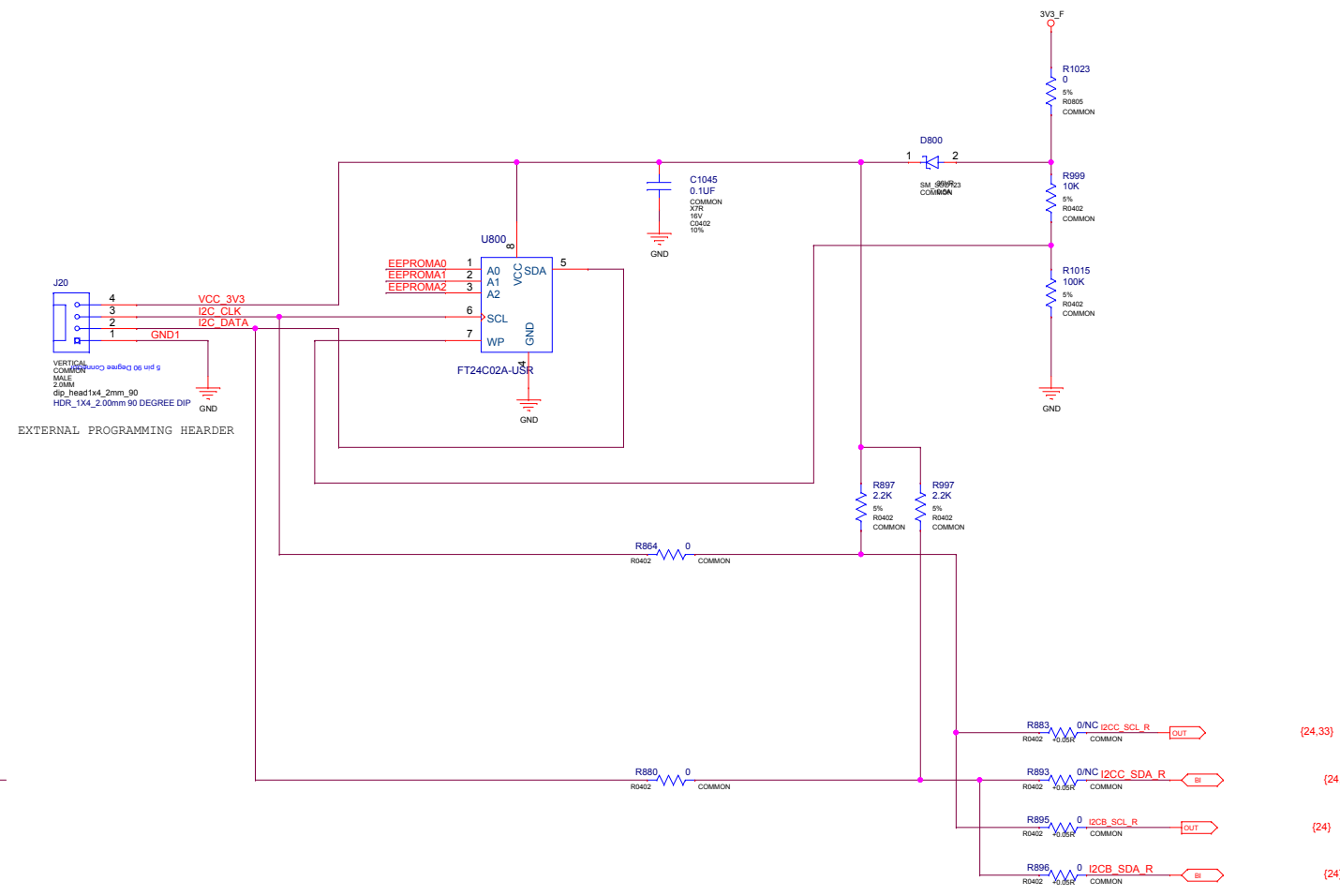
GC6 FB ENABLE



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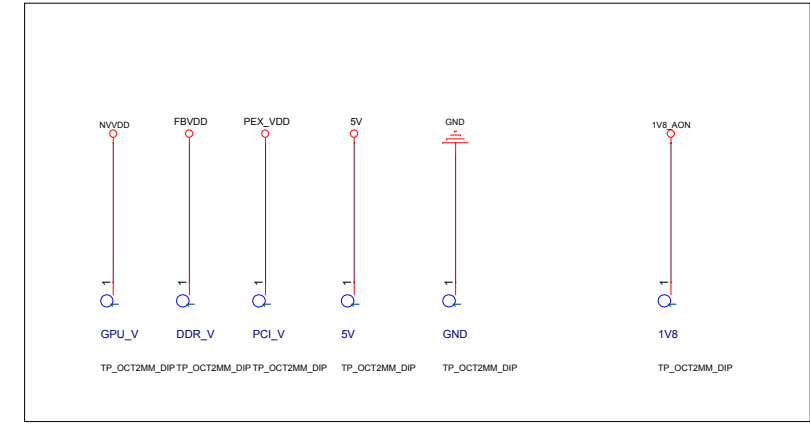
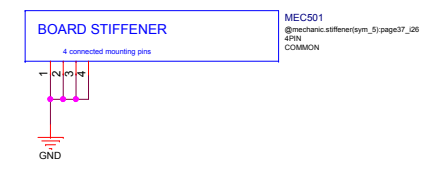
ASSEMBLY PAGE DETAIL	-ASSEMBLY_DESCRIPTION- PS: GC6 MISC
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Page Name: PS: GC6 MISC			
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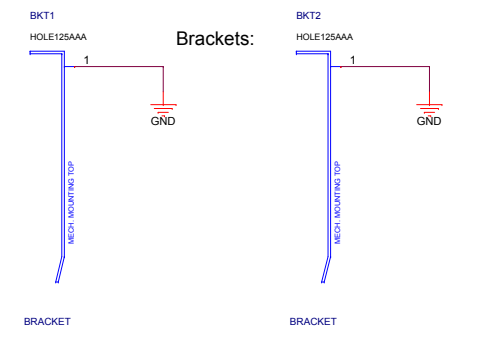


MOUNTING HOLES FOR HS DS:

GPU Stiffener:



MOUNTING HOLES FOR HS SS:



Brackets:

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ASSEMBLY PAGE DETAIL	<ASSEMBLY_DESCRIPTION> MECH
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Page Name: MECH\_SN EEPRON

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