G1 chassis

CIRCUIT DESCRIPTION

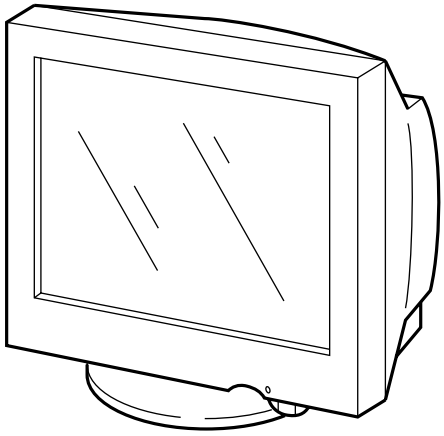


TABLE OF CONTENTS

COLOR GRAPHIC DISPLAY

SONY®

21 inch G1 chassis

1. A BOARD

1-1. VIDEO SELECTOR

This set has input pins of two systems so that the RGB signals of two systems can be received (from two sets of computers). Respective video signals are entered from CN401and 402, and either system is selected by the IC401 (video select IC). The video signals on the selected side are sent to the video amplifier (IC402). This video select IC changes over the output of video signals by the INPUT_SW signal entered from the CN403 pin 12.
In addition, the IC401 has the sync separate function, input signal presence check function, and video out function for the auto size center (ASC). The Sync On G signal is separated by external CR of IC401 pins 27 and 26, and the C. Sync output from pin 25 is buffered in the IC407, then sent to the µ -com from CN403 pin 6. Whether the G-ch signal is entered to either input. 1 or 2 is judged by external CR of IC401 pins 12 and 13, and the output from pin 14 is sent to the µ -com from CN403 pin 7 to be used for recovery from the 1W standby.
The OR of R, G, B signals entered from IC401 pins 19, 21, 23 is converted into the TTL level, and outputted from pin 17, then sent to the IC404 to be used for ASC timing detection.

1-2. VIDEO AMPLIFIER (for instance, Red Channel)

Either one of two-system Red signals entered from CN401 and 402 is selected by the video select IC (see section 1-1), and entered to the pin 2 of video amplifier (IC402). The Red signal is outputted from the IC402 pin 41, and entered to the video pre-main AMP (IC403) pin 12. Video signal amplified by IC403 is outputted from pin 14, and clamped to the controlled DC level at C115 in the cutoff control circuit (see 1-3), then sent to the pin 7 of CRT socket (SK401).
The IC402 is controlled by the built-in D/A converter which makes communication with the µ -com (IC001) on the N Board via I²C. For the brightness only, the DAC output of pin 29 is connected to the control voltage input of pin 34 outside of IC. The DAC outputs of pins 26, 27, 28 are used for R, G, B bias control of user control, the DAC output of pin 25 is used for the reset of IC404.

1-3. CUTOFF CONTROL CIRCUIT

The cutoff control amplifier IC406 is a hybrid IC containing a common base type AMP and a PNP emitter follower. The input pins 13, 14, 15 are clamped to about 5V. The R, G, B back ground control voltage from IC404 and the user control R, G, B bias control voltage from IC402 are composed, then amplified in the IC406. This amplified DC voltage clamps the respective pedestal levels (black level) of R, G, B signals through the clamp diodes (D105, 205, 305). Q401 is a temperature compensator for the IC406.

1-4. G2 CIRCUITS

The G2 control voltage outputted from IC404 pin 14 is entered to the operation AMP (IC405) pin 5 in the G2 AMP circuit consisting of Q410 and IC405. The control voltage amplified by IC405 and Q410 is applied as screen voltage to the CRT socket (SK401) pin 10. Also, Q406, Q407, C436, D405, and D403 compose a spot killer circuit that drops the G2 voltage to the GND level at the power on/off.

1-5. ON-SCREEN DISPLAY (OSD)

This function visually shows the user controls for various setting such as screen size, center, screen distortion, color temperature, etc. on the screen. The pulse signals entered from the CN403 pin 10 (HFBP) and pin 9 (V.SYNC) are entered to the IC404 pin 7 and pin 6 respectively. The FBKG signal synchronizing with these signals are outputted from the IC404 pins 18~21 together with the OSD_R, G, B signals, and entered to the video pre-AMP (IC402) pins 1, 4, 9, 13 respectively. Using the OSD_BLK signal of pin 1, the IC402 replaces original RGB video signals with OSD_RGB signals and outputs them to display the user setting on the screen. Further, the IC404 has the PWM DAC function, ASC timing detecting function, and A/D converter function for the beam current feedback. The PWM DAC function provides four channels to control R, G, B blanking and G2. For the ASC timing detection, the timing of OR (pin 8) of R,G,B signals from IC401 is compared with the timing of H sync (pin 5) and V sync (pin 6) from the N Board, and its result is sent to the µ -com (IC001) via I²C bus. For the A/D converter function, the DC voltage from the beam current detection circuit mentioned later is A/D-converted, and sent to the µ -com (IC001) via I²C bus.
Q402 is for forcible reset of the IC404. When a communication between µ -com (IC001) and IC404 failed, the IC402 pin 25 goes in high status to turn off/on the Q402. As a result, the power for IC404 is turned off/on to reset the IC404.

1-6. BEAM CURRENT DETECTION CIRCUIT (for instance, Red Channel)

Utilizing the fact that the clamp current flowing through the clamp diodes (D105, 205, 305) in the blanking period is proportional to the beam current, the beam current is detected to compensate the cutoff variations of CRT. The clamp current sucked from the clamp diode (D105) into the PNP emitter follower in IC406 comes out of the R_IK (pin 12) as it is. It is transformed into the voltage by R128, then rectified in the D103, R130, C108, and C114. The side of D103 connected to 5 V is for the limit that prevents the beam current detection voltage from exceeding 5 V. After rectification, the beam current detection voltage is buffered in the emitter follower Q101, then entered to the IC404 pin 26.

2. D BOARD

2-1. VERTICAL DEFLECTION CIRCUIT

The vertical sawtooth wave entered from the CN505 pin 1 is amplified by the V-OUT IC (IC701), and outputted as vertical deflection current from pin 2, and supplied to the vertical deflection coil between pins 2 and 3 of CN509.
The vertical deflection current is determined mainly by R723, 724, 725, and 726.

2-2. HORIZONTAL DEFLECTION CIRCUIT

The horizontal screen size control signal entered from CN504 pin 2 and the horizontal screen distortion control signal entered from CN504 pin 1 are added in the IC503, then entered to the IC501 pin 6.
The voltage entered to the IC501 pin 6 is compared with the reference voltage generated by the 9V regulator built in the IC501 and entered to the pin 7, and its difference is outputted from the pin 3 as PWM (pulse width modulation) waveform.
This waveform isentered to the Q508 gate pin via Q504 and Q505 buffers.
The Q508 switches the 220 V power supply voltage entered to the source pin according to the gate voltage, and outputs it to the drain pin. This output voltage is supplied to the Q515 (H-OUT) collector via L505 (HOC).
The horizontal deflection circuit composed of horizontal deflection coils connected to the Q515, D511, C543, and CN509 transforms this voltage into the current, then the current is supplied to the horizontal deflection coils.

2-3. HORIZONTAL DRIVE CIRCUIT

Rectangular wave for horizontal drive entered from the CN505 pin 6 is buffered in Q502 and Q503, then drives the Q509 and T501 (HDT). When Q509 turns on, the current from the base of Q515 (H-OUT) flows from T501 pin 8 to pin 5 via D508 to turn off the Q515. Also, when Q509 turns off, the current flows to the Q515 base via R547 to turn on the Q515.

2-4. HORIZONTAL CENTER CIRCUIT

The H-CENT DC signal entered from the CN504 pin 6 is entered to the horizontal center circuit consisting of Q514 and IC502, and amplified there.
In the same manner, the H-CENT AC signal entered from CN505 pin 4 is entered to the horizontal center circuit and amplified there. These signals are supplied via T502 to the horizontal deflection coils connected to the CN509 as part of horizontal deflection current.

2-5. S-SHAPE CORRECTION CAPACITOR SWITCHING CIRCUIT

Using the TTL signals (S0~S6) turned on/off by the input horizontal deflection frequency, the Q501, Q506, and RY501 switch over the S-shape correction capacitors (C509, C521, etc.) so as to be met with the input horizontal deflection frequency.

2-6. HIGH VOLTAGE GENERATION CIRCUIT

High voltage is divided into 1/3000 in the T902 (FBT), and outputted from the T902 pin 17, and entered to the IC901 pin 11.
The voltage entered to the IC901 pin 11 is compared with the reference voltage generated by the 9V regulator built in the IC901 and entered to the pin 12, and its difference is outputted from the pin 3 as PWM (pulse width modulation) waveform, then entered to the Q905 gate pin.
The Q905 switches the 220 V power supply voltage entered to the source pin according to the gate voltage, and outputs it to the drain pin.
This output voltage is supplied to the Q906 (high voltage converter) drain via T901 (HRC).
On the other hand, based on the rectangular wave for horizontal drive entered from the CN505 pin 6, the rectangular wave for high voltage drive is generated in IC901, and drives the high voltage converter (Q906) via buffer composed of Q903 and Q904.
The resonance circuit consisting of Q906, C916, T902 generates the fly-back pulse signal based on the voltage supplied to the Q906 drain.
This signal voltage is raised by the T902 (fly-back transformer), and high voltage is supplied to the CRT.

2-7. HIGH VOLTAGE PROTECTION CIRCUIT

The pulse voltage where the fly-back pulse is divided is outputted from the T902 (FBT) pin 6, and rectified in D912 and C922.
This rectified voltage rises as high voltage increases, and if high voltage becomes extremely high due to any failure, it turns on Q907 and Q908 via D914 and D915. Further, D921 turns on to drop the voltage waveform entered to the Q906 gate to the ground level. Thus, the Q906 drive stops, and then the high voltage generation circuit stops.

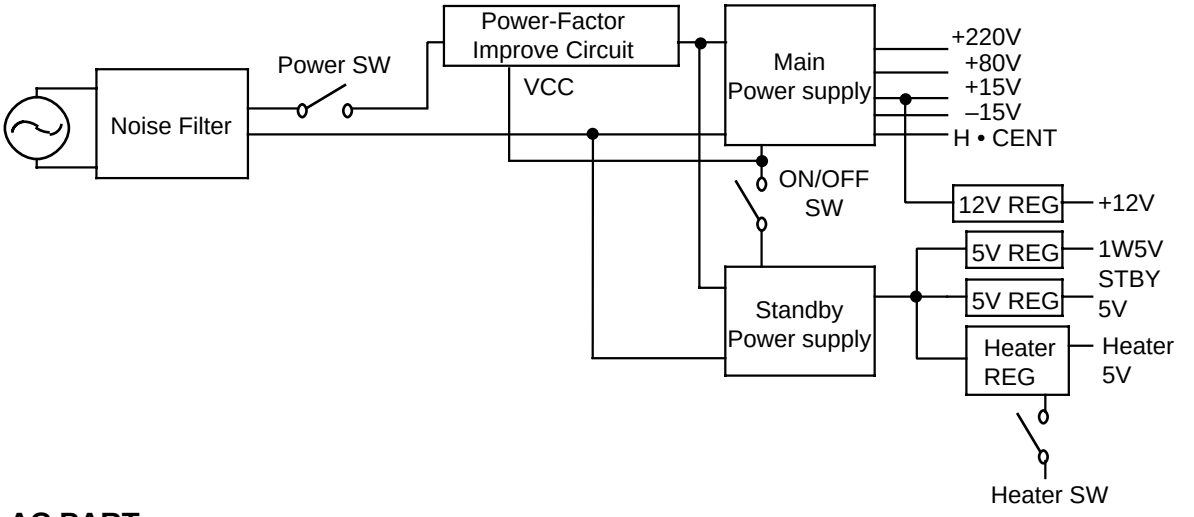
2-8. BEAM CURRENT PROTECTION CIRCUIT

The Zener circuit consisting of D902, R904, and R906 supplies the beam current to the T902 (FBT) pin 11 via R930, R931, and R928.
The voltage at T902 pin 11 is finally entered to the µ -com on N Board via IC503 buffer and CN504 pin 10. When the beam current increases, the voltage at T902 pin 11 drops and also the voltage entered to the µ -com drops. If this voltage drops to 0 V, the µ -com judges that the beam current increases excessively, then it stops the operation of power supply circuit (G Board).

2-9. DYNAMIC FOCUS CIRCUIT

Parabolic signal for vertical dynamic focus entered from the CN504 pin 12 uses as power supply the 400 V DC voltage generated by rectifying the output waveform from T502 pin 6 by the D709 and C703, and it is amplified into 100 V~340 V by Q706 and Q707, then supplied to the T902 pin 15 as vertical dynamic focus voltage.
Also, parabolic signal for horizontal dynamic focus entered from the CN504 pin 14 is amplified into -300 V~+600 V by T701 (DFT) via buffer consisting of Q701~Q705, then supplied to the T902 pin 14 as horizontal dynamic focus voltage.

3. G BOARD



3-1. AC PART

3-1-1. AC Filter

The noise filter consists of AC inlet (with a filter), T601, C601, C602, C603, C604, and C607.
The power thermistor TH601 is used to limit the rush current, and it is shorted by the relay RY602 simultaneously with the main power supply on so that the TH601 also works when the power is turned on again.

3-1-2. Degauss Circuit

The degauss circuit is controlled by the degauss signal from the µ -com. Degauss is executed when the relay RY601 turns on and the damping current flows by the posistor THP601. The varistor VDR601 clamps the degauss voltage so that even the degauss current in AC200 V system is equivalent to that in AC100 V system.

3-2. POWER SUPPLY PART

3-2-1. Standby Power supply Circuit

When AC is entered, the standby power supply turns on to supply the power to the µ -com.
The standby power supply consists of IC630, Q630, T630, etc. and the IC630 is a PWM controller that performs switching at about 110 kHz.
The start current for IC630 flows to the pin 7 by R635 and R602, and after IC630 started, IC630 operates continuously with about 15 V bias voltage generated in the T630 pin 4, while the start current is cut off by Q631 and Q632.
The output voltages are 6.55 V (regulated by IC680 and feed back by PH630) generated in the T630 pin 8 and about 15 V generated in the T630 pin 4.
6.55 V on the secondary side is used for the standby 5 V (IC652), 1W5 V (IC653), heater 5 V (IC651), Main Power SW, and USB power (only for models with USB).
About 15 V on the primary side is used for Vcc of IC630, Vcc of power-factor improve circuit IC610, main power starting, and relay driving for power thermistor.
1W5 V is always outputted while the standby power supply is operating.
Standby 5 V stops at the active off (1W mode) because IC652 pin 1 goes LOW.
Heater 5 V stops at the active off, because IC651 pin 1 goes LOW.
The output voltage is lowered to about 3.5 V at the suspension because Q671 turns on.

3-2-2. Main Power supply

The main power supply circuit is a self-oscillating current resonance type half bridge where the current flows to the T620 ③-④ windings alternately to generate the voltage on the windings on the secondary side by turning on/off alternately two transistors built in the Q603 with the frequency determined by the resonance between C625 and T621 ②-③ windings and C626 and T621 ④-⑤ windings.
The T621 is an orthogonal transformer, and it can vary the inductance of ②-③ windings and ④-⑤ windings on the primary side according to the current flowing to the ⑦-⑧ windings on the secondary side. The control of output voltage is made where the IC650 detects +B voltage and controls the current to the T621 ⑦-⑧ windings to vary the inductance of ②-③ windings and ④-⑤ windings on the primary side so as to vary the switching frequency. Other output voltages are generated respectively according to the winding ratio to the +B output winding.

3-2-3. Power-Factor improve Circuit (Active Filter)

The power-factor improving circuit is a step-up chopper system composed of IC610, L610, etc. where a controller and converter MOSFET, and rectifier diode are built in the IC610.
The AC voltage is rectified by D610, and the energy is stored in L610 when the converter MOSFET turns on, and the energy is superposed in the input voltage to step up the voltage when the converter MOSFET turns off. Thus, the AC voltage is rectified by the rectifier diode, then smoothed by C610.
The built-in controller detects the input voltage, rectified voltage, switching voltage, and L610 voltage respectively to step up the rectified voltage to about 390 V, control the input current to the value proportional to the AC voltage waveform, and control the on/off of MOSFET so as to restrain the generation of harmonic current.
The switching frequency is 50~300 kHz and it varies depending on the input voltage and output load.
This circuit operates only when the main power supply works, and it stops in the power save mode.

3-2-4. Main ON/OFF Circuit

(1) Main ON
When the Power signal goes High, Q652 turns on, and the signal is transmitted to the primary side by the photocoupler PH620. Then, the Q610 turns on, and Vcc is supplied to the IC610 to start the power-factor improving circuit and also to turn off the Q621, and then the start current flows to the base of Q603 to start the main power supply. At this time on the secondary side, Q670 and Q650 turn on to flow the charge current to C663 via T621 ⑦-⑧ windings so as to raise the switching frequency to restrain the rush current at the start. (Soft start of main power supply)
When C663 charging finished, the Q650 turns off and a steady operation is performed.

(2) Main OFF
When the power signal goes low, Q652 turns off, and then the Q651 turns on to discharge the C663 and to turn on the Q650, so that the current flows to the T621 ⑦-⑧ windings to raise the switching frequency so as to reduce the base current of Q603.
At the same time, the signal is transmitted to the primary side by PH620 to turn off the Q610, and Vcc of IC610 is cut off to stop the power-factor improving circuit and also to turn on the Q621 to cut off the drive current to the base of Q603, and then the main power supply stops.

3-2-5. +B Over-voltage Protection Circuit

The +B voltage is detected by R680, 688, 668, and when theR668 voltage reached about 22 V, Q653 and Q667 turn on to make the power switch signal Low so as to stop the main power supply. (Latch circuit)

4. N BOARD

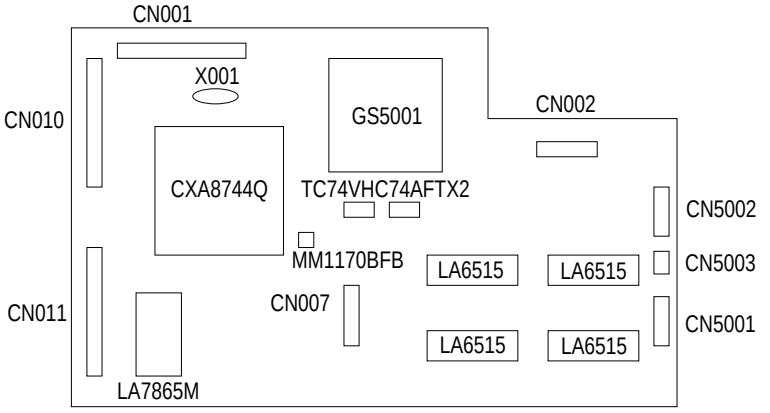
4-1. GENERAL

The N Board has mainly nine functions as listed below:

① System control (microcomputer function)
② Sync check function (SCU) } Integrated in CXD8744Q
③ Deflection control function (DSP)
④ Vertical deflection waveform generation
⑤ Horizontal deflection synchronization } Integrated in LA7865M
⑥ LCC control amplifier (LA6515) x5ch
⑦ Rotation, horizontal and vertical convergence control AMP, (LA6515) x3ch
⑧ Geomagnetic sensor (GS5001)
⑨ 1W detection circuit (TC74VHCT74x2)

These nine functions are mounted in the 245mmx195mm area. FIG.1 shows the arrangement of main components on the N Board.

FIG.1 Arrangement on A side of N Board



4-2. FUNCTIONS AND FUNCTIONAL DESCRIPTION

4-2-1. System Control, Sync Check, and Deflection Control (CXD8744Q)

The IC001 (CXD8744Q) has mainly three functions as mentioned above.

4-2-1-1. IC001 (CXD8744Q) Pin Description

The pin description of IC001 (CXD8744Q) is given in the following tables. <FIG.2>~<FIG.5>

Pin No	Function	Name	Functional Description
1	VPP	VPP	µ -com internal bias output pin
2	MVBIAS	MVBIAS	µ -com internal bias input pin
3	I/O port	LED0	Green LED lighting pin. Hi: LED ON
4	I/O port	LED1	Red LED lighting pin. This becomes amber when ON simultaneously with Green LED.
5	I/O port	HDSW	Hdrive Pulse duty switching output pin
6	I/O port	NC	NC
7	I/O port	NC	NC
8	I/O port	ECO	1W_DET Circuit Start signal output pin
9	I/O port	NC	NC
10	I/O port	NC	NC

<FIG.2>

Pin No	Function	Name	Functional Description
11	I/O port	NC	NC
12	I/O port	NC	NC
13	I/O port	INPUT_SW	Input signal select SW position detect pin
14	I/O port	LoB_DET	LoB detect pin. Lo: Normal operation status
15	I/O port	PRT_DET	No connection (PWR_SW operation detection)
16	I/O port	GND	GND
17	I/O port	GND	NC
18	I/O port	MOIRE_LoFH	Moire frequency select SW. FH<60 kHz:Lo FH>60 kHz:Hiz
19	I/O port	OFF_DET	1 W_DET circuit start detect pin. Lo: Detection of recovery from 1 W
20	VDD	VDD1	Connected to STBY+5 V
21	I/O port	P47	Connected to VDD1
22	I/O port	NC	NC
23	I/O port	NC	NC
24	I/O port	NC	NC
25	I/O port	NC	NC
26	Input port	GND	GND
27	Input port	GND	GND
28	I/O port	DDET1	DDC1 +5 V detection
29	I/O port	HOST G_1	DDC1 GND detection
30	I/O port	DDET2	DDC2 +5 V detection
31	I/O port	HOST G_2	DDC2 GND detection
32	I/O port	GND	GND
33	I/O port	WDP	Watch-dog timer reset signal output pin
34	Input port	RESET	Reset signal input pin from watch-dog timer
35	VDD	VDD2	Connected to STBY+5 V
36	I/O port	GND	GND
37	GND	GND	GND
38	I/O port	SCL1	I²C bus CLK line for EEPROM access
39	I/O port	SDA1	I²C bus DATA line for EEPROM access
40	I/O port	EEPWC	EEPROM Write Control signal output pin
41	I/O port	SCL2	I²C bus CLK line for video device access
42	I/O port	SDA2	I²C bus DATA line for video device access
43	I/O port	NC	NC
44	Input port	RXD	Universal serial communication port, input pin
45	I/O port	TXD	Universal serial communication port, output pin
46	I/O port	DSCL1	I²C bus access CLK line for DDC1
47	I/O port	DSDA1	I²C bus access DATA line for DDC1
48	I/O port	DSCL2	I²C bus access CLK line for DDC2
49	I/O port	DSDA2	I²C bus access DATA line for DDC2
50	GND	GND2	GND
51	Output port	CBLK	Composite blanking pulse output for video pre-AMP
52	Output port	BKGP	Background pulse output for OSD
53	Output port	BKGP	Clamp pulse output for video pre-AMP
54	I/O port	S0	S-shape capacitor select SW. Hi: S-shape capacitor ON
55	I/O port	S1	S-shape capacitor select SW. Hi: S-shape capacitor ON
56	I/O port	S2	S-shape capacitor select SW. Hi: S-shape capacitor ON
57	GND	GND3	GND
58	I/O port	S3	S-shape capacitor select SW. Hi: S-shape capacitor ON
59	I/O port	S4	S-shape capacitor select SW. Lo: S-shape capacitor ON

<FIG.3>

Pin No	Function	Name	Functional Description
60	I/O port	S5	S-shape capacitor select SW. Hi: S-shape capacitor ON
61	I/O port	S6	S-shape capacitor select SW. Hi: S-shape capacitor ON
62	GND	OSCVSS	GND
63	Input port	XTB	Crystal connection pin; input pin
64	Output port	XTO	Crystal connection pin; output pin
65	VDD	OSCVDD	Connected to STBY+5 V
66	I/O port	VSAWRST	Reset pulse output pin for V-shape generation
67	I/O port	VSH	Sample Hold pulse output pin for V-shape generation
68	I/O port	NC	NC
69	I/O port	INPUTSEL	Video Signal Input Select signal output pin. Lo: Input 2 selected
70	GND	GND4	GND
71	DACoutput	HDF	Horizontal dynamic focus output pin
72	GND	AVSS1	GND
73	DACoutput	NC	NC
74	VDD	AVDD1	Connected to STBY+5 V
75	ADCinput	TEMP	Set warming-up time measuring pin after power ON
76	ADCinput	KEY_DET	User key selection detect pin
77	ADCinput	ENV	Set environment (temperature) measuring pin
78	ADCinput	LUMI	Set environment (brightness) measuring pin
79	GND	AVSS2	GND
80	ADCinput	NC	NC
81	ADCinput	NC	NC
82	ADCinput	NC	NC
83	ADCinput	VX	Geomagnetism detect signal input pin; X direction level
84	ADCinput	VY	Geomagnetism detect signal input pin; Y direction level
85	ADCinput	NC	NC
86	ADCinput	HVDET	High voltage (HV) failure detect pin
87	VDD	AVDD2	Connected to STBY+5 V
88	ADCinput	THDET	D Board overheat detect pin (S-shape select SW circuit)
89	ADCinput	ABLDET	ABL detect pin
90	ADCinput	HPLL	Horizontal deflection frequency pulling control pin
91	GND	GND5	GND
92	INT	VRET	Vertical deflection pulse detect pin
93	I/O port	HTR	Heater power ON/OFF pin. Hi: Heater ON
94	I/O port	PWR_SW	Power ON/OFF control pin. Hi: Power ON
95	I/O port	DGS	Degauss control pin. Hi: ON
96	I/O port	AFCSW	Horizontal sync/async, select pin. Hi: Async mode
97	I/O port	HPHASESW	NC
98	I/O port	HSOUT	Hsync output pin
99	I/O port	MOIREPLS	Moire cancel pulse output pin
100	VDD	VDD3	Connected to STBY+5 V
101	VDD	VDD	Connected to STBY+5 V
102	I/O port	CLPDLY	CR mounting pin for clamp pulse generation
103	Input port	VS1	Vsync input pin on input 1 side
104	Input port	HS/CS1	HS/CS input pin on input 1 side
105	GND	GND6	GND
106	Input port	HS/CS2	HS/CS input pin on input 2 side
107	Input port	VS2	Vsync input pin on input 2 side
108	Input port	SOG	Sync Separate signal input pin at sync on green

<FIG.4>

Pin No	Function	Name	Functional Description
109	Input port	HFBP	Fly-back pulse input pin
110	GND	GND7	GND
111	DACoutput	HFREQ	PDM-DAC output pin for horizontal deflection frequency control
112	VDD	VDD5	4.5 V (exclusive for HFREQ)
113	VDD	VDD6	4.5 V (exclusive for HPHASE)
114	DACoutput	HPHASE	PDM-DAC output pin for horizontal deflection phase control
115	GND	GND8	GND
116	GND	GND9	GND
117	DACoutput	DVSHAPE	PDM-DAC output pin for VSHAPE differential waveform output
118	VDD	VDD7	4.5 V (exclusive for DVSHAPE)
119	VDD	VDD8	4.5 V (exclusive for VSHAPLVL)
120	DACoutput	VSHAPLVL	PDM-DAC output pin for VSHAPE amplitude control
121	GND	GND10	GND
122	DACoutput	VDC	PDM-DAC output pin for VSHAPE DC level control
123	GND	GND11	GND
124	DACoutput	MOIRECONT	PDM-DAC output pin for Moire level control
125	VDD	VDD9	Connected to STBY+5 V
126	DACoutput	HSHPBAL	PDM-DAC output pin for HSHAPE balance component control
127	VDD	VDD10	Connected to STBY+5 V
128	DACoutput	VDF	PDM-DAC output pin for V dynamic focus control
129	GND	GND12	GND
130	GND	GND13	GND
131	DACoutput	VCONV	PDM-DAC output pin for V convergence control
132	VDD	VDD11	Connected to STBY+5 V
133	DACoutput	HSP	PDM-DAC output pin for HSHAPE waveform control
134	GND	GND14	GND
135	GND	GND15	GND
136	DACoutput	HSIZE	PDM-DAC output pin for H size control
137	VDD	VDD12	Connected to STBY+5 V
138	DAC output	HCENT	PDM-DAC output pin for H center control
139	VDD	VDD13	Connected to STBY+5 V
140	DACoutput	ROTATION	PDM-DAC output pin for rotation control
141	GND	GND16	GND
142	DACoutput	NSLAND	NC
143	GND	GND17	GND
144	DACoutput	HLINBAL	PDM-DAC output pin for H linearity balance control
145	DACoutput	NC	NC
146	VDD	VDD14	Connected to STBY+5 V
147	VDD	VDD15	Connected to STBY+5 V
148	DACoutput	HCONV	PDM-DAC output pin for H static convergence control
149	DACoutput	LCCNS	PDM-DAC output pin for landing (NS) control
150	GND	GND18	GND
151	GND	GND19	GND
152	DACoutput	LCCLT	PDM-DAC output pin for landing (upper left) control
153	DACoutput	LCCRT	PDM-DAC output pin for landing (upper right) control
154	VDD	VDD16	Connected to STBY+5 V
155	VDD	VDD17	Connected to STBY+5 V

<FIG.5>

Pin No	Function	Name	Functional Description
156	DACoutput	LCCLB	PDM-DAC output pin for landing (lower left) control
157	DACoutput	LCCRB	NC PDM-DAC output pin for landing (lower right) control
158	GND	GND20	GND
159	GND	GND21	GND
160	VDD	VDD18	Connected to STBY+5 V

4-2-1-2. Sync Check Function

With regard to HS/CS, VS, and SOG inputs, HSYNC and VSYNC are generated through the specified selection. The selection matrix is as listed in < FIG.6.>.

(Note: sogdis is a register set by the µ -com for the sync check function.)

HS/CS	VS	HSOUT		VSOUT	
		sogdis=0	sogdis=1	sogdis=0	sogdis=1
×	×	SOG	HS/CS	SOG	VS
×	○	HS/CS		VS	
○	×	HS/CS		HS/CS	
○	○	HS/CS		VS	

<FIG.6>

4-2-1-3. Deflection Control Function

As deflection control signals, the following nine waveforms are generated through the DSP operation, and they can be controlled freely within the specified range. As they are digital outputs, low frequencies are passed with the RC filter to generate analog waveforms. The output waveform names, output pins, and description of output waveforms are as follows.

① DVSHAPE : Pin No.117 : V. deflection differential waveform
② HSHAPE : Pin No.133 : H. deflection corrected waveform
③ HSHPBAL : Pin No.126 : H. deflection balance component corrected waveform
④ VCONV : Pin No.131 : V. convergence corrected waveform
⑤ VDF : Pin No.128 : V. dynamic focus waveform
⑥ ROTATION : Pin No.140 : Rotation. Normally DC
⑦ MOIRECONT : Pin No.124 : Moire level control
⑧ NSLAND : Pin No.142 (No connection)
⑨ HDFAMP : Used internally in IC. Output is superposed in HDF signal.

4-2-1-4. System Control Function

The N Board has nine functions (1)~(9) as mentioned in “1. General”, and these functions are totally controlled by the system control function (µ -com function).
This section describes particularly the protection against the system control failures, as well as the meaning of LED indication.

1) Meaning of LED indicators

The LED indicators display the monitor statuses such as power on, power saving, shut down, etc.
<FIG.7> shows the LED indicators. Also, the failure detect conditions are listed in (1) to (5).

Monitor statuses	LED indicators	Remarks
POWER_ON	Green	
STAND_BY	Amber (0.5 sec) and Green (0.5 sec)	
SUSPEND	Amber (0.5 sec) and Green (0.5 sec)	
ACTIVE_OFF	Amber	
SELF_DOWN	Amber	µ-com is turned off
No Power Supply	Amber (0.5 sec) and Off (0.5 sec)	+15V power is not present
+B_FAILURE	Amber (0.5 sec) and Off (0.5 sec)	+B failure or +B stop
DEF_FAILURE	Amber (0.5 sec) and Off (0.5 sec)	H deflection stop, V deflection stop, or FET overheat
ABL_FAILURE	Amber (0.5 sec) and Off (0.5 sec)	ABL
HV_FAILURE	Amber (0.5 sec) and Off (0.5 sec) and Amber (0.25 sec) and Off (1.25 sec)	Extremely high voltage, or high voltage stop
Aging/Self_test	Amber (0.5 sec) and Off (0.5 sec) and Green (0.5 sec) and Off (0.5 sec)	
Out of scan range	OSD display	

<FIG.7>

Note: In <FIG.7>, the system failures are “No Power Supply”, “+B_FAILURE”, “DEF_FAILURE”, “ABL_FAILURE”, and “HV_FAILURE”. Other indications show normal operation.

① No Power Supply
In monitoring the +15 V line voltage, if a failure is detected (no power supply status continues for more than 2 sec), the system is forcibly shut down. In concrete, Hi or Lo of IC001 pin 14 is detected.

② +B_FAILURE
In monitoring the +B line voltage, if a failure is detected (no power supply status continues for more than 2 sec), the system is forcibly shut down.

③ DEF_FAILURE
If horizontal or vertical deflection stop status continues for more than 2 sec, or if S-shape select FET temperature alarm continues more than 2 sec, the system is forcibly shut down. In concrete, the pulse of pin 109 (HFBP input) and pin 92 (VRET), and the voltage of pin 88 (THDET) are detected.

④ ABL_FAILURE
If ABL detection continues for more than 2 sec, the system is forcibly shut down. In concrete, the potential of pin 89 (ABLDET) is detected.

⑤ HV_FAILURE
If high voltage detection continues for more than 2 sec, or if the voltage value is out of the specified value, the system is forcibly shut down. In concrete, the voltage of pin 86 (HVDET) is detected.

4-2-2. Vertical Deflection Waveform Generation and Horizontal Sync (LA7865M)

The IC010 (LA7865M) has mainly two functions as mentioned previously.

4-2-2-1. IC010 (LA7865M) Pin DescriptionThe following table lists the IC010 (LA7865M) pin description. <FIG.8>

Pin No	Function	Name	Functional Description
1	NC	NC	NC
2	Capacitor Pin	S/H_C	Capacitor pin for VSHAPE AGC
3	DC Output Pin	VCC4.5 V	4.5 V regulator output
4	Pulse Input Pin	VSAWRST	VSHAPE integrator reset pulse input pin
5	Pulse Input Pin	VSH	VSHAPE integrator sample hold pulse input pin
6	Sig Output Pin	VSHAPE	VSHAPE output pin
7	VCC	VCC12	Power supply pin (12 V)
8	Pulse Input Pin	FBP	FBP input pin
9	DC Input Pin	AFC_SW	AFC free run setting pin. Hi: Free run
10	Capacitor Pin	FBP_DLY	Pseudo FBP pulse generation pin
11	Capacitor Pin	FBP_DLY1	FBP delay mono. multi capacitor mounting pin
12	NC	NC	NC
13	DC Output Pin	HPLL	AFC filter voltage output pin
14	DC Input Pin	HD_DUTY	Horizontal deflection drive pulse duty control pin
15	Pulse Output Pin	HD	Horizontal deflection drive pulse output pin
16	VCC	VCC12	Power supply pin (12 V)
17	NC	NC	NC
18	NC	NC	NC
19	NC	NC	NC
20	NC	NC	NC
21	DC Output Pin	REG9 V	9V regulator output pin
22	Capacitor Pin	FILTER	VCO filter mounting pin
23	GND	GND	GND
24	Capacitor Pin	VCO_C	VCO oscillating capacitor mounting pin
25	Capacitor Pin	AFC_FIL	AFC filter mounting pin
26	Resister Pin	IREF_R	Reference current resistor mounting pin
27	DC Input Pin	HFREQ	Horizontal deflection frequency control pin
28	Capacitor Pin	HSDLY	HSYNC delay mono. multi capacitor mounting pin
29	DC Input Pin	HPHASE	Horizontal deflection phase control pin
30	Pulse Input Pin	HS	HSYNC pulse input pin
31	GND	GND	GND
32	Capacitor Pin	VSHP_C	VSHAPE integrator capacitor mounting pin
33	DC Input Pin	VDC	VSHAPE DC level control pin
34	DC Input Pin	DVSHAPE	VSHAPE differential waveform input pin

<FIG.8>

4-2-2-2. Vertical Deflection Waveform Generation

IC010 generates the VSHAPE waveform using “DVSHAPE:34pin”, “VDC:33pin”, “VSHPLVL:35pin” signals entered from IC001 (CXD8744Q) and two timing pulses “VSH:5pin”, “VSAWRST:4pin”.

The DVSHAPE signal outputted from IC001 is a differential waveform on the premise that it is integrated completely in the IC010. Complete integration of this DVSHAPE signal in the IC010 generates a slope of V period that follows the DVSHAPE signal. Also, the VSAWRST puls is provided for rapid discharge of capacitor (C067) that generatthis slope.

Further, the VSHPLVL signal is provided to control and maintain the VSHAPE amplitude level. For this amplitude control, AGC type controlsystem is employed where the VSH pulse is used to detect the amplitude. The IC010 pin 2 is the AGC hold capacitor mounting pin, where C078: 0.22 µF is mounted. The vicinity of this capacitor is a very sensitive.

The DC level control of VSHAPE is made with the DC level of VDC signal (pin 33).

4-2-2-3. Horizontal Deflection Synchronization

This section describes another function of IC010, horizontal deflection synchronizing circuit. The AFC operation of IC010 is a one-loop type PLL. Therefore, the HSYNC pulse which is a sync pulse and the FBP pulse which is an async pulse are synchronized at the delayed timing in the delay circuit in IC010. The phase control signal is entered from the pin 29 to control the delay amount in the delay circuit.

Also, the fo control signal which is HSYNC frequency is entered from the pin 27. This control signal controls the internal VCO of IC010 so as to vary the fo. The frequency lock is checked by making the AFCSW (pin 9) Hi and measuring the free run frequency of VCO to confirm that it accords with the HSYNC frequency, or by measuring the voltage of AFCFIL (pin 25). In the case of AFCFIL (pin 25) voltage measurement, the potential is 2.5 V (DC) when the frequency is locked.

4-2-2-4. Additional IC010 Functions

The IC010 provides a 9 V shunt type regulator and a 4.5 V regulator that divides 9V voltage by 2. The 4.5 V regulator output is supplied to the part of PDM-DAC of IC001 (DVSHAPE, VSHPLVL, VDC, HFREQ, HPHASE) to cancel the temperature characteristics in combination with the IC010.

4-2-3. LCC Control AMP (LA6515)

The IC5301, IC5101, and IC5201 (1/2) on the N Board compose the LCCcontrol amplifier. LA6515 (no fins) is a successor of LA6510, and functional performance is same. The control of CLL control amplifier is made with the DC voltage supplied from the IC001.

4-2-4. Rotation, Horizontal & Vertical Convergence Control AMP

(LA6515)The IC5201 (1/2) and IC5401 on the N Board compose the rotation, horizontal and vertical convergence control amplifier. The rotation and horizontal convergence control is made with the DC voltage, while the vertical convergence control is made with the dynamic waveform of V period outputted from the CXD8744Q.

4-2-5. Geomagnetic Sensor (GS5001)

The geomagnetic sensor (GS5001) is a Hi-IC on the sub-board. The geomagnetism detected by the geomagnetic sensor on the sub-board is amplified and outputted. Based on this value, the µ -com calculates the direction of set and performs the rotation, landing correction, and V center correction properly.

The output of geomagnetic sensor is entered to the IC001 pins 83 and 84.

4-2-6. 1W Detection Circuit (IC004, IC005, Q004~Q007)

If no signal is entered with the POWER SW turned on, the set goes in the power save mode called 1W mode following the DPMS. Under this condition, a part of power supply circuit, input signal detection circuit, and 1W detection circuit are operating. The transition to this power save mode and its reset are executed as follows.

When the µ -com confirms that no signal is entered, it turns on the latch circuit consisting of Q005 and Q006, and turns off the power supply including the µ-com itself, except the power supply for the power saving. This state is the 1W mode. As for the reset of 1 W mode, when a signal was entered, the power supply including the µ -com turn on by the “ECO-SW” signal outputted from the IC004, IC005 pins 5 and 9, then the µ -com determines the set condition.

4-2-7. WDT (IC002)

The IC002 is a watch-dog timer. It provides the following functions:

1) Generation of the reset pulse at power on
2) Detection of a short break of power supply voltage
3) Watch-dog timer function

Under normal condition, the µ -com always generates the reset cancel signal to the IC002, and accordingly the IC002 does not generate the reset signal to the µ -com. However, if the µ -com cannot generate the reset cancel signal where the µ -com internal conditionis not determinate such as at power on, the IC002 generates the reset signal to the µ -com. As a result, the µ -com is reset.

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